PATENT ABSTRACTS OF JAPAN

(11)Publication number :   2003-150104

(43)Date of publication of application : 23.05.2003

(51)Int.Cl.	G09G 3/30
	G09F 9/30
	G09G 3/20
	H05B 33/14

(21)Application number : 2001-349888

(22)Date of filing :   15.11.2001

(71)Applicant : MATSUSHITA ELECTRIC IND CO LTD

(72)Inventor : TAKAHARA HIROSHI

(54) METHOD FOR DRIVING EL DISPLAY DEVICE, AND EL DISPLAY DEVICE AND INFORMATION DISPLAY DEVICE

(57)Abstract:
PROBLEM TO BE SOLVED: To provide an EL display device without dispersion in brightness in a display plane.
SOLUTION: In each pixel, a TFT 11a1 and a TFT 11a2 for driving use are formed. The two TFT 11a share a gate terminal. The current Iw from a source signal line 18 is programmed in a capacitor 19. In a 1st firld, a TFT 11f1 is brought into ON sate, and a current Idd1 is made to flow through an EL element 15. The EL element emits light with brightness corresponding to Idd1. In a 2nd field, a TFT 11f2 is brought into ON state, and a current Idd2 is made to flow through the EL element 15. The EL element 15 emits light with brightness corresponding to Idd2. Since a program current is Iw=Idd1+Idd2, an average light emitting brightness of the EL element 15 in the two fields corresponds to a half of the program current Iw.
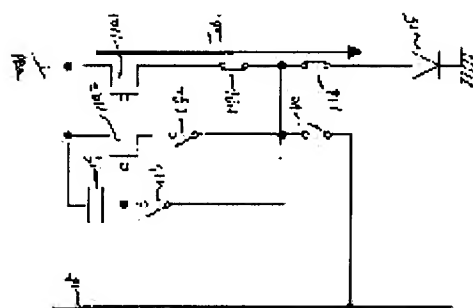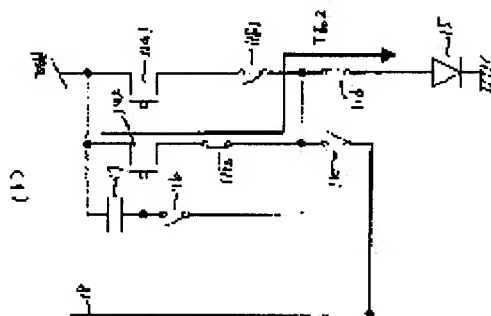
LEGAL STATUS

[Date of request for examination]

[Date of sending the examiner's decision of rejection]

[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]

[Date of final disposal for application]

[Patent number]

[Date of registration]

[Number of appeal against examiner's decision of rejection]

[Date of requesting appeal against examiner's decision of rejection]

[Date of extinction of right]

JP 2003-150104 English Translation

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] EL display panel of this invention which displays an image mainly with spontaneous light -- and it is related with information displays, such as a cellular phone using these EL display panels, etc.
[0002]
[Description of the Prior Art] Since many liquid crystal display panels to a portable equipment etc. are adopted from the advantage of a low power with the thin shape, they are used for devices, such as a word processor, and a personal computer, television (TV), the viewfinder of a video camera, a monitor, etc.
[0003]
[Problem(s) to be Solved by the Invention] However, since a liquid crystal display panel is not a spontaneous light device, it has the trouble that it cannot be displayed that an image does not use a back light. Since predetermined thickness was required in order to constitute a back light, there was a problem that the thickness of a display module became thick. Moreover, in order for a liquid crystal display panel to perform color display, it is necessary to use a color filter. Therefore, there was a trouble that efficiency for light utilization was low. It is shown in EL display and is [0004].
[Means for Solving the Problem] In order to solve the above-mentioned technical problem, this invention is an EL display which a pixel is arranged in the shape of a matrix, and is characterized by the drive transistor component which impresses a current, the capacitor which carries out predetermined period maintenance of the gate terminal voltage of said drive transistor component, and the switching element which short-circuits the both ends of said capacitor being formed by the EL element and said EL element at said each pixel.
[0005]
[Embodiment of the Invention] In order that each drawing may make a plot easy easily [understanding] in this specification, there are an abbreviation or/and a part which carried out enlarging or contracting. For example, with the sectional view of the display panel of drawing 7, the closure film 73 etc. is illustrated sufficiently thickly. Moreover, in drawing 1, the thin film transistor (TFT) which impresses a signal to a pixel electrode is omitted. Moreover, it is desirable to omit the phase films for phase compensation etc. and for ** to add timely in the display panel of this invention. The above thing is the same also to the following drawings. Moreover, the part which attached the same number or the notation has a same or similar gestalt, an ingredient, a function, or actuation.
[0006] In addition, especially the contents explained with each drawing etc. are combinable with other examples etc., even if there is no notice. For example, a touch panel etc. can be added to the display panel of drawing 1, and it can consider as drawing 19 and the drawing 49 information display. Moreover, a magnifying lens can be attached and viewfinders (refer to drawing 45), such as a video camera (refer to drawing 44), can also be constituted. Moreover, the drive approach of this invention explained in drawing 31, drawing 51, drawing 104, drawing 106, etc. is applicable to which display or display panel of this invention. Moreover, it cannot be overemphasized that it cannot be limited to this although this invention mainly explains the active-matrix mold display panel with which TFT was formed in each pixel, and it can apply also to a simple matrix type.
[0007] Thus, even if not illustrated especially in the specification, the matter indicated or explained in the specification and the drawing, contents, and a specification can be combined

mutually, and can be indicated to a claim. It is because it is impossible to describe all combination on specifications etc.

[0008] It is a low power, and is high display quality, and the organic electroluminescence display panel constituted as a display panel in which thin-shape-izing is still more possible by arranging the plurality of an organic electroluminescence (EL) component in the shape of a matrix attracts attention.

[0009] As an organic electroluminescence display panel is shown in drawing 4, the laminating of the organic stratum functionale (EL layer) 47 of at least one layer which consists of an electron transport layer, a luminous layer, an electron hole transportation layer, etc. on the glass plate 49 (array substrate) with which the transparent electrode 48 as a pixel electrode was formed, and the metal electrode (reflective film) 46 is carried out. The organic stratum functionale (EL layer) 47 emits light by applying the electrical potential difference of minus to the anode plate (anode) of a transparent electrode (pixel electrode) 48 in the cathode (cathode) of plus and a metal electrode (reflector) 46, namely, impressing a direct current between a transparent electrode 48 and a metal electrode 46. By using the organic compound which can expect a good luminescence property for the organic stratum functionale, EL display panel can be equal to practical use.

[0010] In addition, a cathode electrode, an anode electrode, or the reflective film may form and constitute the optical interference film which becomes an ITO electrode from dielectric multilayers. Dielectric multilayers form the dielectric film of a low refractive index, and the dielectric film of a high refractive index in a multilayer by turns. That is, it is a dielectric mirror. These dielectric multilayers have the function which makes good the color tone of the light emitted from organic electroluminescence structure (screen effect). In addition, other ingredients, such as IZO, are sufficient as ITO. This matter is the same also to a pixel electrode.

[0011] A big current flows for the wiring 51 and 63 which supplies a current to an anode or a cathode. For example, if the screen size of EL indicating equipment turns into 40 inch size, an about [100A] current will flow. Therefore, it is necessary to produce the resistance of these wiring sufficiently low. By this invention, wiring of an anode etc. is first formed with a thin film to this technical problem. And the thickness of a conductor is thickly formed in this thin film wiring with the electrolysis plating technique. Moreover, metal wiring which turns into the wiring itself or wiring from **** is added if needed.

[0012] Moreover, in order to supply a big current to an anode or cathode wiring, it wires from a current supply source means to near, such as said anode wiring, with the power wiring of a small current by the high voltage, and the low battery and the high current are converted the power and supplied using a DC-DC converter etc. That is, it wires from a power source to a power consumption object with the high voltage and small current wiring, and changes into a high current and a low battery near [for power consumption]. A DC-DC converter, a transformer, etc. are illustrated as such a thing.

[0013] It is desirable to use for a metal electrode 46 what has small work functions, such as a lithium, silver, aluminum, magnesium, an indium, copper, or each alloy. It is desirable to use for example, an aluminum-Li alloy especially. Moreover, a conductive big ingredient or gold of a work function, such as ITO, etc. can be used for a transparent electrode 48. In addition, when gold is used as an electrode material, an electrode will be in a translucent condition. In addition, other ingredients, such as IZO, are sufficient as ITO. This matter is the same also to a pixel electrode.

[0014] In addition, in case a thin film is vapor-deposited to the pixel electrode 46 etc., it is good to form the organic electroluminescence film in argon atmosphere. Moreover, by forming the carbon film by 20 or more nm [50] or less on ITO as a pixel electrode 46, the stability of an interface improves and luminescence brightness and luminous efficiency will

also become good.

[0015] Moreover, it cannot be overemphasized that it may not limit to forming EL film by vacuum evaporationo, and you may form by the ink jet.

[0016] Hereafter, in order to make easy an understanding of EL display-panel structure of this invention, the manufacture approach of the organic electroluminescence display panel of this invention is explained first.

[0017] In order to improve heat dissipation nature of a substrate 49, you may form with sapphire glass. Moreover, a good thermally conductive thin film or a thermally conductive good thick film may be formed. For example, using the substrate in which diamond thin films (DLC etc.) were formed is illustrated. Of course, a quartz-glass substrate and a soda glass substrate may be used. In addition, what used ceramic substrates, such as an alumina, used the metal plate which consists of copper etc., or coated [spreading / vacuum evaporationo or] the insulator layer with the metal membrane may be used. When using a pixel electrode as a reflective mold, since outgoing radiation of the light is carried out from the direction of a front face of a substrate as a substrate ingredient, in addition to the transparence thru/or translucent ingredient of glass, a quartz, resin, etc., impermeable material, such as stainless steel, can also be used. This configuration is illustrated to drawing 7. The cathode electrode is formed with the transparent electrodes 72, such as ITO.

[0018] In addition, although [the example of this invention] a cathode etc. is formed by the metal membrane, it may not limit to this and you may form by transparent membranes, such as ITO and IZO. Thus, a transparence EL display panel can be constituted by using the anode of EL element 15, and the electrode of both cathodes as a transparent electrode. By gathering permeability to about 80%, without using a metal membrane, displaying an alphabetic character and a picture, it can constitute so that the other side of a display panel may almost be transparent and it may be visible.

[0019] It cannot be overemphasized that a substrate may use a plastic plate. A plastic plate cannot break easily, and since it is lightweight, it is the optimal as a substrate for display panels of a cellular phone. As for a plastic plate, it is desirable to stick an auxiliary substrate on one field of the base substrate used as a core material with adhesives, and to use as a laminated circuit board. Of course, these substrate 321 grades may not be limited to a plate, and a with a 0.3mm or less 0.05mm or more thickness film is sufficient as them.

[0020] As a substrate of a base substrate, it is desirable to use alicyclic polyolefin resin. A single plate with a thickness [of ARTON by Japan Synthetic Rubber Co., Ltd.] of 200 micrometers is illustrated as such alicyclic polyolefin resin. The auxiliary substrate (or a film or film) which consists of polyester resin, polyethylene resin, or polyether sulphone resin etc. with which the rebound ace court layer which has thermal resistance, solvent resistance, or a moisture permeability-proof function in one field of a base substrate, and the gas barrier layer with an infiltrative-proof function were formed is arranged.

[0021] When it constitutes a substrate 49 from plastics as mentioned above, a substrate 49 consists of a base substrate and an auxiliary substrate. The auxiliary substrate (or a film or film) which consists of polyether sulphone resin with which the rebound ace court layer and the gas barrier layer were formed in the field of another side of a base substrate like the above-mentioned is arranged. It is desirable to make it the include angle of the optical lagging axis of an auxiliary substrate and the optical lagging axis of an auxiliary substrate to make turn into 90 degrees. In addition, a base substrate and an auxiliary substrate are stuck through adhesives or a binder, and let them be a laminated circuit board.

[0022] It is desirable to use what consists of resin acrylic in UV (ultraviolet rays) hardening mold as adhesives. Moreover, as for acrylic resin, it is desirable to use what has a fluorine radical. In addition, the adhesives or the binder of an epoxy system may be used. As for the refractive index of adhesives or a binder, it is desirable to use or more 1.47 1.54 or less thing.

Moreover, it is desirable to make it a refractive-index difference with the refractive index of a substrate 49 become 0.03 or less. especially -- adhesives -- previously -- written **** -- it is desirable to add optical dispersing agents, such as titanium oxide [like], and to make it function as a light-scattering layer.

[0023] In case an auxiliary substrate and an auxiliary substrate are stuck on a base substrate, it is desirable to make into 120 or less degrees the include angle which the optical lagging axis of an auxiliary substrate and the optical lagging axis of an auxiliary substrate make 45 degrees or more. It is good to make it still more desirable 100 or less degrees 80 degrees or more. By making it this range, the phase contrast generated by the polyether sulphone resin which is an auxiliary substrate and an auxiliary substrate can be completely negated within a laminated circuit board. Therefore, the plastic plate for display panels can be treated now as an isotropic substrate without phase contrast. Therefore, the nonuniformity of the display panel by phase conditions differing does not occur with the configuration which used the circular polarization of light plate.

[0024] By this configuration, versatility spreads remarkably compared with a film substrate with phase contrast, or a film laminated circuit board. That is, it is because the linearly polarized light can be changed into elliptically polarized light by combining a phase contrast film as a design. If there is phase contrast in a substrate 49 etc., an error with a design value will occur according to this phase contrast.

[0025] Here, as a rebound ace court layer, polyester resin, epoxy system resin, urethane system resin, or acrylic resin can be used, and the 1st under coat layer of the transparence electric conduction film is served both as a stripe-like electrode or a pixel electrode.

[0026] Moreover, as a gas barrier layer, organic materials, such as inorganic materials, such as SiO_2 and SiO_x, or poly vinyl alcohol, and polyimide, etc. can be used. As a binder, adhesives, etc., epoxy system adhesives or polyester system adhesives can be used other than the acrylic described previously. In addition, thickness of a glue line is set to 100 micrometers or less. However, in order to graduate the irregularity of front faces, such as a substrate, it is desirable to be referred to as 10 micrometers or more.

[0027] Moreover, it is desirable to use a with a 40-micrometer or more thickness [400 micrometer] thing as the auxiliary substrate which constitutes a substrate 49, and an auxiliary substrate. Moreover, the unevenness or phase contrast at the time of melting extrusion molding called the die line of polyether sulphone resin can be low suppressed by setting thickness of an auxiliary substrate and an auxiliary substrate to 120 micrometers or less. Preferably, thickness of an auxiliary substrate is set to 50 micrometers or more 80 micrometers or less.

[0028] Next, SiO_x is formed in this laminated circuit board as an auxiliary under coat layer of the transparence electric conduction film, and the transparence electric conduction film which consists of ITO which serves as a pixel electrode if needed is formed with a spatter technique. Moreover, the ITO film is formed as a static free if needed. Thus, the transparence electric conduction film of the manufactured plastic plate for display panels can realize sheet resistance 25ohm/**, and 80% of permeability as the film property.

[0029] 50 to 100 micrometers when thin, in the production process of a display panel, the plastic plate for display panels will curl [the thickness of a base substrate] by heat treatment. Moreover, a good result is not obtained in connection of passive circuit elements. When a base substrate is made into 500 micrometers or less in 200-micrometer or more thickness with a single plate, there is no deformation of a substrate and it excels in smooth nature, and conveyance nature is good and is stabilized by the transparence electric conduction film property. Moreover, connection of passive circuit elements can also be made satisfactory. Furthermore, especially thickness has 250 micrometers or more good 450 micrometers or less. It thinks because it has moderate flexibility and smoothness. In addition, other ingredients,

such as IZO, are sufficient as ITO. This matter is the same also to a pixel electrode.

[0030] In addition, when using organic materials, such as the above-mentioned plastic plate, as a substrate 49, it is desirable to form the thin film which consists of an inorganic material as a barrier layer also in the field which touches a light modulation layer. As for the barrier layer which consists of this inorganic material, it is desirable to form with the same ingredient as an AIR coat. In addition, it cannot be overemphasized that the closure substrate 41 as well as a substrate 49 is producible with a technique or a configuration.

[0031] Moreover, when forming the barrier film on a pixel electrode or a stripe-like electrode, in order to reduce the loss of the electrical potential difference impressed to a light modulation layer as much as possible, it is desirable to use a low dielectric constant ingredient. For example, the amorphous carbon film (specific inductive capacity 2.0-2.5) which added the fluorine is illustrated. In addition, the LKD series (LKD-T200 series (specific inductive capacity 2.5-2.7), LKD-T400 series (specific inductive capacity 2.0-2.2)) which JSR is manufacturing and selling is illustrated. LKD series is the spin spreading form which used MSQ (methy-silsesquioxane) as the base, and its specific inductive capacity is also low [as 2.0-2.7] desirable. In addition, inorganic materials, such as organic materials, such as polyimide, urethane, and an acrylic, and SiNx, SiO2, are sufficient. It cannot be overemphasized that these barrier film ingredients may be used for an auxiliary substrate.

[0032] By using the substrate 49 formed with plastics, or 41, the advantage not breaking that-izing can be carried out [lightweight] can be demonstrated. There is also another advantage that press working of sheet metal can be carried out. That is, the substrate of the configuration of arbitration is producible with press working of sheet metal or cutting (see drawing 25). Moreover, the configuration of arbitration and thickness are processible with fusion or chemicals processing. For example, forming circularly, making it globular forms (curved surface etc.), or processing it in the shape of a cone is illustrated. Moreover, by press working of sheet metal, irregularity 252 can be formed in one substrate side, and formation of the diffusing surface or embossing can be performed to manufacture and coincidence of a substrate.

[0033] Moreover, it is also easy to form in the hole of the substrate 41 formed by carrying out press working of sheet metal of the plastics so that the gage pin of a back light or a covering substrate can be inserted. Moreover, electrical circuits, such as a substrate 49, a capacitor formed by the thick-film technique or the thin film technology in 41, or resistance, may be constituted. Moreover, by forming a crevice (not shown) in a substrate 41, forming heights 251 in a substrate 49, and forming so that these crevice and heights can be inserted in exactly, you may constitute so that a substrate 41 and a substrate 49 can be unified by fitting.

[0034] When a glass substrate was used, the bank used in case EL is vapor-deposited to the periphery of a pixel 16 was formed. A bank (rib) is formed in the shape of heights using a resin ingredient by 1.0-micrometer or more thickness of 3.5 micrometers or less. It forms in 1.5-micrometer or more height of 2.5 micrometers or less still more preferably. ******** -- the bank (heights) 251 which consists of resin -- formation of substrates 41 or 49 -- simultaneously, it is also producible. In addition, an SOG ingredient besides acrylic resin and polyimide resin is sufficient as a bank ingredient. In case a bank carries out press working of sheet metal of a substrate 41 or the substrate 49, it forms the heights 251 of resin in coincidence (see drawing 25). This is big effectiveness generated by forming substrates 41 and 49 by resin.

[0035] Thus, since production time can be shortened by forming the resin section in a substrate and coincidence, low-cost-izing is possible. Moreover, heights 251 are formed in the viewing-area section in the shape of a dot at the time of manufacture of a substrate 49 etc. These heights 251 are good to form between contiguity pixels. These heights 251 hold the predetermined space of a substrate 41 and a substrate 49. The shape of a stripe besides the

shape of ** which encloses a pixel electrode has as the shape of a soil note.

[0036] In addition, although [the above example] the heights 251 which function as a bank are formed, it does not limit to this. For example, it is good also as investigating a picture element part by press working of sheet metal etc. (crevice). In addition, formation forms the concave heights 252 and heights 251 in a substrate and coincidence, and also a flat surface substrate is formed first and the method which presses by reheating and forms irregularity is contained after that.

[0037] Moreover, a mosaic-like color filter may be formed by coloring substrates 41 and 49 directly. Techniques, such as ink jet printing, are used for a substrate, and a color, coloring matter, etc. are applied and are made to permeate. What is necessary is to make it dry at an elevated temperature after osmosis, and just to cover a front face with inorganic materials, such as resin, such as UV resin, silicon oxide, or nitrogen oxide. Moreover, a color filter is formed with the semi-conductor pattern formation technique of applying and developing the film with a gravure technique, an offset-printing technique, and a spinner etc. A black matrix (BM) may be directly formed by being [it / using a technique / in the relation between others, black or the dark color, or the complementary color of the light to modulate]-similarly coloring. [color filter] Moreover, a crevice may be formed so that it may correspond to a pixel in a substrate side, and you may constitute so that a color filter, BM, or TFT may be embedded in this crevice. It is desirable to carry out the coat especially of the front face with acrylic resin. With this configuration, there is also an advantage that flattening of the pixel electrode surface etc. is carried out.

[0038] Moreover, the resin on the front face of a substrate may be electric-conduction-ized by a conductive polymer etc., and a pixel electrode or a cathode electrode may be constituted directly. A hole is made in a substrate still more greatly and the configuration which inserts electronic parts, such as a capacitor, in this hole is also illustrated. The advantage which a substrate can constitute thinly is demonstrated.

[0039] Moreover, a pattern may be freely formed by cutting the front face of a substrate. Moreover, you may form by melting the periphery of substrates 41 and 49. Moreover, in the case of an organic electroluminescence display panel, the periphery of a substrate may be melted and closed in order to prevent penetration of the moisture from the outside.

[0040] As mentioned above, punching processing to a substrate is easy by forming a substrate by resin. Moreover, press working of sheet metal etc. can constitute a substrate configuration freely. Moreover, a hole can be made in substrates 41 and 49, this hole can be filled up with electric conduction resin etc., and it can also be made to flow through the table and flesh side of a substrate electrically. Substrates 41 and 49 can use as a multilayered circuit board or a double-sided substrate.

[0041] Moreover, a current-carrying pin etc. may be inserted instead of electric conduction resin. You may constitute so that the terminal of electronic parts, such as a capacitor, can be fitted over the formed hole. Moreover, circuit wiring by the thin film, a capacitor, a coil, or resistance may be formed in a substrate. That is, it is good also considering a substrate 41 and 49 self as a multilayer wiring substrate. Multilayering consists of those of making a thin substrate rival. One or more of the substrates (film) to stretch may be colored.

[0042] Moreover, a color and coloring matter are added to a substrate ingredient, it can be colored the substrate itself or a filter can be formed. Moreover, a serial number can also be formed in substrate production and coincidence. Moreover, it can prevent malfunctioning from that of light being irradiated by loaded IC chip by coloring only parts other than a viewing area.

[0043] Moreover, the one half of the viewing area of a substrate can also be colored a different color. This should just apply resin plate processing techniques (injection processing, comp REKUSHON processing, etc.). Moreover, one half of a viewing area can also be made

into different EL layer membrane thickness from that of using the same processing technique. Moreover, a display and the circuit section can also be formed in coincidence. Moreover, it is also easy to change the substrate thickness of a viewing area and a driver loading field.

[0044] Moreover, a micro lens can also be formed so that it may correspond to a pixel, or so that it may correspond to a substrate 41 or a substrate 49 at a viewing area. Moreover, a diffraction grating may be formed by processing substrates 41 and 49. Moreover, irregularity more detailed enough than pixel size is formed, an angle of visibility can be improved or an angle-of-visibility dependency can be given. In addition, processing of such an arbitration configuration, ultra-fine processing technology, etc. are realizable with the La Stampa technique which OMRON Corp. developed and which carries out micro-lens formation.

[0045] As for substrates 41 and 49, the stripe-like electrode (not shown) is formed. An antireflection film (AIR coat) is formed in the field where a substrate touches air. When the polarizing plate etc. is not stuck on substrates 41 and 49, an antireflection film (AIR coat) is directly formed in substrates 41 and 49. When other components, such as a polarizing plate (polarization film), are stuck, an antireflection film (AIR coat) is formed in the front face of the component etc.

[0046] In addition, although it explained as a core that substrates 41 and 49 formed the above example with plastics, it does not limit to this. For example, even if substrates 41 and 49 are a glass substrate and a metal substrate, press working of sheet metal, cutting, etc. can form or constitute the concave heights 252, heights 252, etc. Moreover, the coloring to a substrate etc. is possible. Therefore, the explained matter is not limited to a plastic plate. Moreover, it does not limit to a substrate, either. For example, a film or a sheet is sufficient.

[0047] Moreover, in order to prevent or control adhesion of the contaminant to the front face of a polarizing plate, it is effective to form the thin film which consists of a fluororesin. Moreover, conductor film, such as a thin film which has a hydrophilic group for electrostatic prevention, conductive polymer film, and a metal membrane, may be applied or vapor-deposited.

[0048] In addition, the polarizing plate (polarization film) arranged or formed in the optical plane of incidence or the optical outgoing radiation side of a display panel 82 may not be limited to what is made into the linearly polarized light, and may serve as elliptically polarized light. Moreover, two or more polarizing plates may be stretched, a polarizing plate and a phase contrast plate may be combined, or what was stretched may be used.

[0049] As a main ingredient which constitutes a polarization film, a TAC film (triacetyl cellulose film) is the optimal. A TAC film is because it has the outstanding optical property, surface smooth nature, and processing suitability.

[0050] The configuration which forms an AIR coat by dielectric monolayer or multilayers is illustrated. In addition, the resin of a low refractive index of 1.35-1.45 may be applied. For example, the acrylic resin of a fluorine system etc. is illustrated. Or more 1.37 1.42 or less thing of a refractive index is [especially a property] good.

[0051] Moreover, an AIR coat has the configuration of three layers, or a two-layer configuration. In addition, in the case of three layers, it is used in order to prevent reflection in the wavelength band of the large light. This is called a multi-coat. In a two-layer case, it is used in order to prevent reflection in the wavelength band of the specific light. This is called V quart. A multi-coat and V quart are properly used according to the application of a display panel. In addition, not the thing to limit more than two-layer but one layer is sufficient.

[0052] In the case of a multi-coat, optical thickness carries out $nd1 = lambda / 4$ laminatings of $nd1 = lambda/2$ and the magnesium fluoride (MgF_2) for $nd = lambda/4$, and a zirconium (ZrO_2), and an aluminum oxide (aluminum $2O_3$) is formed. Usually, a thin film is formed as a value of 520nm or near of those as lambda.

[0053] optical in silicon monoxide (SiO) in the case of V quart -- $nd1 = lambda / 4$ laminatings

of nd1=lambda/4 or yttrium oxide (Y2O3), and the magnesium fluoride (MgF2) are carried out, and thickness nd1=lambda/4, and magnesium fluoride (MgF2) are formed. It is better to use Y2O3, when modulating blue glow, since SiO has an absorption band region in a blue side. Moreover, since the direction of Y2O3 is stable also from the stability of the matter, it is desirable. Moreover, SiO2 thin film may be used. Of course, it is good also as an AIR coat using the resin of a low refractive index etc. For example, acrylic resin, such as a fluorine, is illustrated. As for these, it is desirable to use an ultraviolet curing type.

[0054] In addition, in order to prevent that static electricity is charged by the display panel, it is desirable that a hydrophilic property consists of good ingredients into substrate ingredients, such as to apply the resin of a hydrophilic property to front faces, such as light guide plates, such as a covering substrate, and a display panel 82, or a panel.

[0055] The thin film transistor (TFT) as two or more switching elements or current controlling elements is formed in 1 pixel. TFT to form may be TFT of the same class, and like TFT of a P channel mold and N channel mold, although you may be TFT of a different class, a switching transistor and the transistor for a drive of the thing of like-pole nature are desirably desirable. Moreover, the structure of TFT is not limited by TFT of a planar mold, and may also depend that in which a stagger mold or a reverse stagger mold may be used, and the impurity range (the source, drain) was formed using the self aryne method on a non-self aryne method.

[0056] The EL display device 15 of this invention has EL structure by which the laminating of ITO and one or more sorts of organic layers used as a hole impregnation electrode (pixel electrode), and the electron injection electrode was carried out one by one on the substrate. TFT is prepared in said substrate.

[0057] In order to manufacture EL display device of this invention, the array of TFT is first formed on a substrate at a desired configuration. And by the spatter, membranes are formed and patterning of the ITO which is a transparent electrode as a pixel electrode on the flattening film is carried out. Then, the laminating of an organic electroluminescence layer, the electron injection electrode, etc. is carried out.

[0058] What is necessary is just to use the usual polycrystalline silicon TFT as TFT. TFT is prepared in the edge of each pixel of EL structure, and the magnitude is about 10-30 micrometers. In addition, the magnitude of a pixel is about 20micrometerx20micrometer-300micrometerx300micrometer.

[0059] The wiring electrode of TFT is prepared on a substrate. There is a function for a wiring electrode to have low resistance, to connect a hole impregnation electrode electrically, and to hold down resistance low, and generally, that wiring electrode is not restricted to this ingredient in this invention, although the thing containing any one sort of aluminum, aluminum and transition metals (however, Ti is removed), Ti, or the titanium nitride (TiN) or two sorts or more is used. What is necessary is just to usually set it to about 100-1000nm as thickness of the whole which combined the hole impregnation electrode and the wiring electrode of TFT used as the substrate of EL structure, although there is especially no limit.

[0060] An insulating layer is prepared between the wiring electrode of TFT11, and the organic layer of EL structure. Insulating layers may be any as long as the paint film of resin system ingredients, such as what formed inorganic system ingredients, such as silicon oxide of SiO2 grade and silicon nitride, with a spatter or vacuum deposition, a silicon oxide layer which formed by SOG (spin-on glass), a photoresist, polyimide, and acrylic resin, etc. has insulation. Polyimide is desirable especially. Moreover, an insulating layer also plays the role of the anticorrosion and the waterproof film which protects a wiring electrode from moisture or corrosion.

[0061] The luminescence peak of EL structure may be two or more. EL display device of this invention being green and a blue light-emitting part are obtained with the combination of EL

structure of bluish green color luminescence for example, and a green transparency layer or a blue transparency layer. A red light-emitting part can be obtained by the fluorescence conversion layer which changes bluish green luminescence of EL structure of bluish green color luminescence, and this EL structure into the wavelength near red.

[0062] Next, EL structure which constitutes the EL display device 15 of this invention is explained. EL structure of this invention has the electron injection electrode which is a transparent electrode, one or more sorts of organic layers, and a hole impregnation electrode. An organic layer has at least one-layer hole transportation layer and a luminous layer, respectively, for example, has an electron injection transportation layer, a luminous layer, an electron hole transportation layer, and a hole injection layer one by one. In addition, there may not be a hole transportation layer. The organic layer of EL structure of this invention can be considered as various configurations, and electron injection and a transportation layer may be omitted, it may consider as a luminous layer and one, or it may mix a hole-injection transportation layer and a luminous layer. An electron injection electrode consists of the small metal, compound, or alloys of the work function preferably formed with vacuum deposition, such as vacuum evaporationo and a spatter.

[0063] Especially ITOIZO is desirable, although ITO (tin dope indium oxide), IZO (zinc dope indium oxide), ZnO, SnO2, and In2O3 grade are mentioned since it is the structure which takes out the light which emitted light from the hole impregnation electrode side as a hole impregnation electrode for example. As for the thickness of a hole impregnation electrode, it is [that what is necessary is just to have the thickness more than / which can perform hole impregnation enough / fixed] usually desirable to be referred to as about 10-500nm. Although it is required for driver voltage to be low in order to raise the dependability of a component, ITO of 10-30ohms / ** (50-300nm of thickness) is mentioned as a desirable thing. When actually using it, the cross protection by reflection by hole impregnation electrode interfaces, such as ITO, should just set up the thickness and the optical constant of an electrode so that optical ejection effectiveness and color purity may fully be satisfied.

[0064] Although a hole impregnation electrode can be formed with vacuum deposition etc., forming by the spatter is desirable. What is necessary is not to restrict and just to use inert gas, such as Ar, helium, Ne, Kr, and Xe, or these mixed gas especially as sputtering gas.

[0065] An electron injection electrode consists of the small metal, compound, or alloys of the work function preferably formed with vacuum deposition, such as vacuum evaporationo and a spatter. In order to raise metallic element simple substances, such as K, Li, Na, Mg, La, Ce, calcium, Sr, Ba, aluminum, Ag, In, Sn, Zn, and Zr, or stability as a component of the electron injection electrode formed, it is desirable to use the alloy system containing them of two components and three components. As an alloy system, Ag-Mg (Ag:1 - 20at%), aluminum-Li (Li:0.3 - 14at%), In-Mg (Mg:50 - 80at%), aluminum-calcium (calcium:5 - 20at%), etc. are desirable, for example.

[0066] What is necessary is just to set preferably 0.1nm or more of thickness of an electron injection electrode thin film to 1nm or more that what is necessary is just to consider as the thickness more than [which can perform electron injection enough] fixed. Moreover, although there is especially no limit in the upper limit, thickness is just usually about 100-500nm.

[0067] A hole injection layer has the function which makes easy impregnation of the electron hole from a hole impregnation electrode, and an electron hole transportation layer has the function which bars the function and electron which convey an electron hole, and is also called a charge impregnation layer and a charge transportation layer.

[0068] An electron injection transportation layer is prepared when the electron injection transportation function of the compound used for a luminous layer is not so high, and it has the function which bars the function which makes easy impregnation of the electron from an

electron injection electrode, the function to convey an electron, and an electron hole. A hole injection layer, an electron hole transportation layer, and an electron injection transportation layer increase - Make the electron hole and electron which are poured in to a luminous layer shut up, make a recombination field optimize, and improve luminous efficiency. In addition, an electron injection transportation layer may be separately prepared in a layer with an impregnation function, and a layer with a transportation function.

[0069] Although the thickness of a luminous layer, the thickness which combined the hole injection layer and the electron hole transportation layer, and especially the thickness of an electron injection transportation layer are not limited but it changes also with formation approaches, it is usually desirable to be referred to as about 5-100nm.

[0070] What is necessary is just to make them into comparable as the thickness of a luminous layer or 1 / about 10 to 10 times, although the thickness of a hole injection layer and an electron hole transportation layer and the thickness of an electron injection transportation layer are based on the design of recombination / luminescence field. As for an impregnation layer, it is [each thickness in the case of dividing the thickness of a hole injection layer and an electron hole transportation layer, and an electronic injection layer and an electron transport layer] desirable to set 1nm or more and a transportation layer to 20nm or more. The upper limit of the thickness of the impregnation layer at this time and a transportation layer is usually about 100nm in an impregnation layer in about 100nm and a transportation layer. It is also the same as when preparing two layers of impregnation transportation layers about such thickness.

[0071] Moreover, taking into consideration the carrier mobility and the carrier consistency (decided by ionization potential and the electron affinity) of the luminous layer and electron injection transportation layer to combine, or a hole-injection transportation layer, by controlling thickness, it is possible to design a recombination field and a luminescence field freely, and design of the luminescent color, control of the luminescence brightness and emission spectrum by the cross protection of two electrodes, and control of the spatial distribution of luminescence are enabled.

[0072] The luminous layer of EL element 15 of this invention is made to contain the fluorescence matter which is the compound which has a luminescence function. Bluish green color luminescent material which is indicated by metal complex coloring matter, such as tris (8-quinolinolato) aluminum [Alq3] which is indicated by JP,63-264692,A etc., JP,6-110569,A (phenyl anthracene derivative), a 6-114456 official report (tetra-aryl ethene derivative), JP,6-100857,A, this JP,2-247278,A, etc. as this fluorescence matter, for example is mentioned.

[0073] The organic EL device 15 of blue luminescence is good to use for the ingredient of a luminous layer "DMPhen (Triphenylamine)" whose luminescence wavelength is about 400nm. Under the present circumstances, it is desirable that a band gap adopts the same ingredient as a luminous layer as an electronic injection layer (Bathocuproine) and a hole injection layer (m-MTDATXA) in order to raise luminous efficiency. Only by a band gap using 3.4eV and large DMPhen for a luminous layer, it is because an electron remains in an electronic injection layer, an electron hole remains in a hole injection layer and recombination of an electron and an electron hole cannot happen easily due to a luminous layer. The luminescent material equipped with an amine radical like DMPhen moves the energy excited in DMPhen to a dopant to the technical problem that structure is unstable and cannot carry out reinforcement easily, and can be solved by making light emit from a dopant.

[0074] As an EL ingredient, luminous efficiency can be improved by using phosphorescence luminescent material. The external quantum efficiency of a firefly luminescence ingredient is about 2 - 3%. Since phosphorescence luminescent material reaches to about 100% to the internal quantum efficiency (effectiveness which changes the energy by excitation to light) of

a firefly luminescence ingredient being 25%, external quantum efficiency becomes high.
[0075] It is good for the host ingredient of the luminous layer of an organic EL device to use CBP. The photoluminescence ingredient which does not green (G) and blue (B) blue [red (R), and] Get here is doped. All the doped ingredients contain Ir. Btp2Ir (acac) and G ingredient are [R ingredient] good for 2(ppy) Ir (acac) and B ingredient to use FIrpic.
[0076] Moreover, the various organic compounds indicated by JP,63-295695,A, JP,2-191694,A, JP,3-792,A, JP,5-234681,A, JP,5-239455,A, JP,5-299174,A, JP,7-126225,A, JP,7-126226,A, JP,8-100172,A, and EP0650955A1 grade can be used for a hole injection layer and an electron hole transportation layer. It is desirable to use a vacuum deposition method for formation of a hole-injection transportation layer, a luminous layer, and an electron injection transportation layer, since a homogeneous thin film can be formed.
[0077] Hereafter, it explains in more detail about the manufacture approach of EL display panel of this invention, and structure. As explained above, TFT11 which drives a pixel to the array substrate 49 is formed first. One pixel consists of four pieces or five TFT(s). Moreover, the current program of the pixel is carried out and the programmed current is supplied to EL element 15. Usually, the value by which the current program was carried out is held as an electrical-potential-difference value at storage capacitance 19. Pixel configurations, such as this combination of TFT11, are explained later. Next, the pixel electrode as a hole-injection electrode is formed in TFT11. The pixel electrode 48 is patternized with photolithography. In addition, in order to prevent image quality degradation by a phot conductor phenomena (it is henceforth called contest a phot) generated by carrying out optical incidence to the lower layer of TFT11, or the upper layer at TFT11, a light-shielding film is formed or arranged.
[0078] in addition, a current program impresses a program current to a pixel from the source driver circuit 14 (or the source driver circuit 14 from a pixel -- absorbing), and makes the signal value equivalent to this current hold to a pixel The current corresponding to this held signal value is passed to EL element 15 (or it slushes from EL element 15). That is, the current which programs with a current and carries out considerable (correspondence) to the programmed current is passed to EL element 15.
[0079] On the other hand, an electrical-potential-difference program impresses a program electrical potential difference to a pixel from the source driver circuit 14, and makes the signal value equivalent to this electrical potential difference hold to a pixel. The current corresponding to this held electrical potential difference is passed to EL element 15. That is, it programs on an electrical potential difference, and an electrical potential difference is transformed into a current value within a pixel, and the current which carries out considerable (correspondence) to the programmed electrical potential difference is passed to EL element 15.
[0080] What is necessary is to use the pentacene molecule which consists of carbon and hydrogen, and just to form an electronic thin film by processing the front face which forms an organic semiconductor, in order to form TFT in a plastic plate. This thin film possesses sufficient semi-conductor property suitable for electron device manufacture while having one 100 times [20 to] the magnitude of the conventional crystal grain of this.
[0081] In case pentacene grows on a silicon substrate, it has the inclination to adhere to a surface impurity. For this reason, growth becomes irregular and it becomes the crystal grain which is too small for manufacturing the device of high quality. In order to grow up crystal grain more greatly, it is good to apply first the monolayer "a molecule buffer" of the molecule called a cyclohexene on a silicon substrate. For a wrap reason, the clean surface can do "sticky sites (location which is easy to adhere)" on silicon, and this layer grows up to be even crystal grain with very big pentacene.
[0082] By using the thin film of such big new crystal grain, the flexible transistor (TFT) using the pentacene of large-sized crystal grain is producible. A transistor (TFT) can be

manufactured by applying a liquefied ingredient at temperature low for mass production method of such a flexible transistor.

[0083] Moreover, after forming on a substrate at the metal thin film and island shape used as the gate and vapor-depositing or applying the amorphous silicon film on this, it may heat and the semi-conductor film may be formed. The semi-conductor film crystallizes good into the part formed in island shape. Therefore, mobility becomes good.

[0084] It is desirable to adopt the structure called a static induction transistor (SIT) as an organic transistor (TFT). The pentacene of an amorphous condition is used. The mobility of an electron hole is lower than 1x10cm2/Vs and the crystallized pentacene. However, frequency characteristics can be raised by adopting SIT structure. As for the thickness of pentacene, it is desirable to be referred to as 100 or more nm [300].

[0085] moreover, organic -- p mold field-effect transistor is sufficient as TFT. TFT can be formed on a plastic plate. Since bending the whole plastic plate is possible, as for the pentacene which can constitute a flexible TFT mold display panel, considering as a polycrystal condition is desirable. It is desirable to use PMMA for the ingredient of gate dielectric film. A naphthacene may be used for the barrier layer of an organic transistor.

[0086] If the oxygen plasma and O2 Usher are used at the time of washing, ashing also of the flattening film 71 of the periphery of the pixel electrode 48 will be carried out to coincidence, and the periphery of the pixel electrode 48 will be scooped out. In order to solve this technical problem, in this invention, the edge protective coat 81 which consists pixel electrode 48 periphery of acrylic resin as drawing 8 shows is formed. The ingredient same as a component of the edge protective coat 81 as organic materials which constitute the flattening film 71, such as acrylic resin and polyimide resin, is illustrated, in addition inorganic materials, such as SiO2 and SiNx, are illustrated. In addition, it cannot be overemphasized that you may be aluminum 2O3 etc.

[0087] The edge protective coat 81 is formed so that after the patterning 48 of the pixel electrode 48 and between the pixel electrode 48 may be filled. Of course, it cannot be overemphasized that it is good also as a bank 3661 (spacer with which it is made for a metal mask not to touch the pixel electrode 48 directly) of the metal mask at the time of forming this edge protective coat 81 in or more 2 height of 4 micrometers or less, and distinguishing an organic electroluminescence ingredient by different color with.

[0088] Moreover, it is effective also in enlarging the pixel electrode 48 so that it may illustrate to drawing 366 improving luminous efficiency. Drawing 366 forms the bank 3661 which makes an edge protective coat serve a double purpose around the pixel electrode 48. A bank 3661 is formed in or more 2 height of 4 micrometers or less. A bank 3661 functions as a spacer it is made not to touch the metal mask (not shown) pixel electrode 48 at the time of distinguishing an organic electroluminescence ingredient by different color with directly.

[0089] In this invention illustrated to drawing 366, the 2nd pixel electrode 3662 is formed in a bank 3661 in piles again at the pixel electrode 48. In the 2nd pixel electrode 3662, it is formed with the same ingredient as the pixel electrode 48. Of course, an ingredient may be changed. As for the 2nd pixel electrode, the pixel electrode 48 and electrical installation are taken. Moreover, it is formed in a bank 3661 in piles. Therefore, a pixel numerical aperture becomes high.

[0090] EL film (47R (red), 47G (green), 47B (blue)) is formed on this 2nd pixel electrode 3662. Each EL film opens few clearances, and is formed, or piles up a periphery. The piled-up part hardly emits light. Moreover, the aluminum film used as a cathode is formed on the EL film 47. In addition, in drawing 366, the 2nd electrode is used as a reflector and, originally it is good also considering the reflective film 46 as a transparent electrode. That is, it is light top ejection.

[0091] With the configuration of drawing 366, the slant face of a bank 3661 is used as pixel

opening. Therefore, since the current density impressed to EL film can be fallen and luminescence area becomes large, effectiveness becomes good (a pixel numerical aperture improves sharply).

[0092] The method which raises hereafter the ejection effectiveness of the light generated within other EL display panels is explained. Drawing 279 explains the technical problem of the conventional EL display. In drawing 279, 2791 is illustrating the locus of light.

[0093] The light generated by the EL film 47 carries out reflection etc. with a cathode 46, and carries out outgoing radiation from the substrate 49 with which the driver circuit 12 (14) was formed. Outgoing radiation of the light which carried out incidence of this optical 2791a at an angle of predetermined to the interface of a substrate 49 and air is carried out from a substrate 49. However, total reflection of the optical 2791b which carried out incidence the include angle beyond the critical angle theta will be carried out within a substrate 49. This optical 2791b that carried out total reflection is reflected irregularly within a substrate 49, and reduces display contrast.

[0094] Optical 2791b which carried out total reflection is lost. The rate of light used as this loss amounts to two thirds of the amounts of total luminous flux which EL element 15 generates. Therefore, reducing generating of optical 2791b links with improvement in the rate for Mitsutoshi directly.

[0095] The configuration which solves this technical problem is a configuration of drawing 280. The refraction sheet (an optical refraction member or optical refraction plate) is attached on the closure film 73 explained by drawing 7 etc. (it arranged or forms). The refraction section 2801 is formed on a triangle, a polygon, or radii so that the refraction sheet 2801 may correspond to a pixel 16. This refraction section 2801 may form the reflective film in the part (inside of the refraction section 2802) which the whole may constitute from a transparence member and is shown by a of drawing 280. The interference film constituted by forming the dielectric film of a low refractive index besides metal membranes, such as aluminum and silver, and the dielectric film of a high refractive index in a multilayer is sufficient as the reflective film. Moreover, a configuration may be set up so that it may become a total reflection field by the Snell's law.

[0096] Moreover, a flection 2802 may be directly formed not only in the configuration which attaches what formed the flection 2802 in the refraction sheet on the closure film 73 but in the closure film 73. Moreover, in the case of the bottom ejection of light, substrate 49 self may be processed, and it may form a flection 2802. Moreover, you may form or arrange on a closure plate.

[0097] Moreover, the configuration of a flection 2802 may not be limited the shape of a slant face, and in the shape of radii, and the shape of a polygon and a screen has as it. Moreover, much needlelike projections crowded and could be formed. Moreover, a flection 2802 is based on being formed in the periphery of the light-emitting part of a pixel 16. That is, if the numerical aperture of a pixel 16 is 30%, it will form in the nonluminescent section (that is, 70% of part) of a pixel 16. Of course, it cannot be overemphasized that the formation location of a flection 2802 may lap with a luminescence location.

[0098] In addition, although a flection 2802 is based on being formed in the periphery of the light-emitting part of a pixel 16, it is desirable to change the center section of the viewing area 21 somewhat by the periphery. In the center section of the viewing area 21, a flection 2802 is formed so that it may be arranged exactly at the periphery of the light-emitting part of a pixel 16. In the periphery of a viewing area 21, it forms so that a flection 2802 may be shifted and arranged outside from the center position of the light-emitting part of a pixel 16 (formation). Thus, by changing the formation location of a flection 2802 by the center section and periphery of a viewing area, generating of moire can be controlled and generating of color nonuniformity can be controlled.

[0099] Moreover, also by forming the location of a flection 2802 in random somewhat for every pixel, generating of moire can be controlled and generating of color nonuniformity can be controlled.

[0100] Moreover, you may constitute so that the light which emitted light by EL element 15 may pass through the interior of a flection 2802, and it may be refracted by this flection 2802 and outgoing radiation may be carried out to the front face of a panel. That is, a flection 2802 acts as prism. In this case, a flection 2802 needs to consist of light transmission material.

[0101] When a flection 2802 forms with a light transmission ingredient, it is effective to color this ingredient. It is because the effectiveness of the color filter which cuts the band of the light emitted from EL element 15 can be demonstrated. Therefore, the color purity of EL display panel improves and a white balance also becomes good. Moreover, when EL element 15 is white luminescence, a color filter cannot be prepared but this flection 2802 can be utilized as a color filter. Of course, it cannot be overemphasized that the flection 2802 which formed the color filter separately and was colored further may be formed or arranged. Moreover, a flection 2802 or the refraction sheet 2801 may be colored directly. Moreover, a flection 2802 or the refraction sheet 2801 may be formed at the charge of a coloring matter.

[0102] As a coloring matter, what distributed coloring matter or a pigment in resin may be used, and gelatin and casein may be dyed by acid dye like a color filter. Fluoran system coloring matter can be made to be able to color and can also be used. Moreover, what is necessary is just to use one or more colors of the arbitration instead of what needs three colors of RGB. Moreover, natural resin can be dyed using coloring matter. Moreover, the ingredient which distributed coloring matter in synthetic resin can be used. Two or more kinds of combination is sufficient as the range of selection of coloring matter in [those] one suitable sort from azo dye, anthraquinone dye, phthalocyanine dye, triphenylmethane dye, etc.

[0103] As for the component of a flection 2802 and the refraction sheet 2801, it is desirable to use a polymer (2861). As a polymer (2861), photo-curing type resin is used from points, such as an ease of a production process, and separation with a liquid crystal phase. The acrylic monomer which ultraviolet-rays hardenability acrylic resin is illustrated as a concrete example, and carries out polymerization hardening especially by UV irradiation, and the thing containing acrylic oligomer are desirable. The photoresist acrylic resin which has a fluorine radical especially has little aging, and its lightfastness is also good.

[0104] As a giant-molecule formation monomer which constitutes a polymer (2861), 2-ethylhexyl acrylate, 2-hydroxyethyl acrylate, a neopentyl glycol door chestnut rate, a hexandiol JIAKU lied, diethylene glycol diacrylate, tripropylene glycol diacrylate, polyethylene-glycol diacrylate, trimethylolpropane triacrylate, pentaerythritol acrylate, etc. are **.

[0105] As oligomer or a prepolymer, polyester acrylate, epoxy acrylate, polyurethane acrylate, etc. are mentioned.

[0106] A polymerization initiator may be used in order to perform a polymerization promptly. Moreover, as this example 2-hydroxy - 2-methyl-1-phenyl propane-1-ON ("DAROKYUA 1173" by Merck Co.), 1-(4-isopropyl phenyl)-2-hydroxy-isobutane-1-ON ("DAROKYUA 1116" by Merck Co.), 1-BIDOROKISHI cyclohexyl phenyl ketone ("IRGACURE 184" by the tiba guy key company), benzyl methyl ketal ("IRGACURE 651" by Ciba-Geigy), etc. are hung up. In addition, a chain transfer agent, a photosensitizer, a color, a cross linking agent, etc. can be suitably used together as an arbitration component.

[0107] In addition, the matter about the above polymer (2861) is applied mainly by the manufacture approach of drawing 286, drawing 287, and drawing 290. In the manufacture approach of drawing 288, a flection 2802 is formed with an inorganic material. Of course, it may be the case of drawing 288 or you may form with an organic material like a polymer.

[0108] Arrangement of a flection 2802 is good to make it the shape of 6 square shapes so that

it may illustrate to drawing 281. Of course, eight or more square shapes etc. are sufficient. A flection 2802 is formed in the perimeter of the light-emitting part of a pixel 16. Even when EL display panel is observed by considering as 6 square-shape configuration as mentioned above, and changing the view which sees the display screen, generating of color nonuniformity and a color shift can lessen very much. Moreover, there are also little luminescence location of a pixel 16 and generating of the moire by location gap of a flection 2802.

[0109] Drawing 281 was the example of a configuration (vertical stripe configuration) of having arranged the same color in the vertical direction of Screen 21. By forming color arrangement of a pixel in the shape of a mosaic, as shown in drawing 282 (arrangement), even if it is a case with comparatively few dots which constitute a display panel, the resolution of the direction of slant of an image improves.

[0110] Moreover, two or more flections 2802 may be formed or arranged to one pixel 16 so that it may illustrate to drawing 283. In the example of drawing 283, the pixel 16 has one pixel electrode and three flections 2801 (2801a, 2801b, 2801c) are formed to this one pixel electrode (arrangement). Of course, it has two or more pixel electrodes in one pixel 16, and a flection 2801 may form to each pixel electrode, respectively (arrangement). In addition, even if it divides a pixel electrode into plurality to one pixel electrode, the decline in a numerical aperture is seldom produced. It is because TFT for a drive or switching etc. is arranged to the periphery of a pixel electrode.

[0111] Of course, one flection 2802 may be arranged to one pixel 284 so that it may illustrate to drawing 284 (formation). moreover, it illustrates to drawing 285 (a) -- as -- one pixel -- two trains -- and the flection 2802 of plurality (drawing 285 (a) 2x six pieces) may be formed. Moreover, as shown in drawing 285 (b), two or more (drawing 285 (b) three pieces) flections 2802 of the shape of a polygon, such as six square shapes, may be formed at one pixel electrode.

[0112] Hereafter, the manufacture approach which forms a flection 2802 (the refraction sheet 2801 may be included) is explained.

[0113] Drawing 286 is the 1st example of this invention. First, the EL film 47 is formed in the substrate 49 with which 11 pixel TFT16, a driver circuit 12-14, etc. were formed. Formation may form the low-molecular EL film by vacuum evaporationo, and may form the macromolecule EL film by the ink jet method. An electrode is formed on the EL film 47 and the closure film 73 is formed on this (drawing 286 (a)). Moreover, a closure plate may be attached. About these matters, since other parts explain to a detail, it omits here.

[0114] Moreover, the manufacture approach indicated on the specifications of this invention is applied except the matter explained below. Moreover, it cannot be overemphasized that it is applied to the following manufacture approaches or the manufactured panel also about the configuration of EL element 15, a pixel configuration, an array configuration, a panel configuration, the drive approach, a drive circuit, etc. Moreover, it cannot be overemphasized that an information display, television, a monitor, a camera, etc. can be constituted using the panel manufactured by the following manufacture approaches, either.

[0115] Next, as shown in drawing 286 (b), a non-hardened BORIMA ingredient (transparent membrane 2861) is applied on the closure film 73. As a polymer ingredient 2861, it is the ingredient of the refraction section 2802 explained previously. In addition, spreading may use which approaches (technique), such as offset printing, screen-stencil, spreading with a roller, and spreading with a spinner.

[0116] Predrying is put in and carried out to oven after spreading of the non-hardened polymer ingredient 2861. Or a taper (ultraviolet rays (UV) and the light are sufficient) is irradiated at a polymer 2861, and the fluidity of the polymer ingredient 2861 is suppressed. Then, it pushes against a transparent membrane 2861, rotating the roller 2862 in which the

configuration of the refraction section 2802 was formed. Thus, the shape of toothing of a roller 2862 is imprinted to a transparent membrane 2861. The irregularity (crevice) 2863 which is equivalent to a transparent membrane 2862 at the refraction section 2801 makes it form by this imprint. UV or the light is irradiated after formation of the concave heights 2863 at the transparent membrane 2861 whole, and a transparent membrane 2861 is stiffened completely.

[0117] The temperature control when carrying out the polymerization of the transparent membrane 2861 is important. Warming is carried out just over or below 60 degrees 40 degrees or more. Although ultraviolet rays (UV) are based also on spectral distribution, they carry out a grade exposure for 8 seconds from 2 seconds by the reinforcement of 20 to about [30mW //cm] two. Such temperature and the exposure conditions of ultraviolet rays must be defined in consideration of the add-in material of a transparent membrane 2861 etc. A front face becomes cloudy when conditions are unsuitable. Moreover, it becomes concave convex [detailed]. In this invention, the ultrahigh pressure mercury lamp was used for the light source at the temperature of 50 degrees C, ultraviolet rays (exposure reinforcement in a substrate side: 30 mW/cm2) were irradiated for 6 seconds at the transparent membrane 2861, and the transparent membrane 2861 was stiffened.

[0118] In addition, the source of luminescence of ultraviolet rays (UV2902) is arranged inside a roller 2862, UV may be irradiated and a transparent membrane 2861 may be made it to carry out sequential hardening in accordance with advance of a roller 2862. Moreover, the generation source of UV2902 is separately prepared with a roller 2862, UV may be irradiated and a transparent membrane 2861 may be made it to carry out sequential hardening from this generation source in accordance with advance of a roller 2862. Moreover, the reflective film etc. is formed in the required part of a flection 2802. About the configuration of the reflective film, since drawing 280 explained, it omits.

[0119] Moreover, the refraction section 2802 may be formed by the manufacture approach of drawing 290. Since drawing 290 (a) and (b) are the same as that of drawing 286 (a) and (b), they omit explanation. In drawing 290 (c), La Stampa 2901 (press plate) which consists of a transparent material is used. The irregularity of the refraction section 2802 and an opposite configuration is formed in the press plate 2901. The press plate 2901 is formed from transparent materials, such as quartz glass. The irregularity of the press plate 2901 is imprinted by the transparent membrane 2861 by pushing this press plate 2901 against a transparent membrane 2861.

[0120] Thus, the shape of toothing of the press plate 2901 is imprinted to a transparent membrane 2861. The irregularity (crevice) 2863 which is equivalent to a transparent membrane 2862 at the refraction section 2801 makes it form by this imprint. UV or the light 2902 is irradiated through the press plate 2901, and the transparent membrane 2861 whole is made to harden a transparent membrane 2861 completely after formation of the concave heights 2863.

[0121] It is desirable to form in the concave convex of the press plate 2901 the good film of the mold releasability which consists of an ingredient of the Ole Von system etc. By forming the good thin film of such mold releasability in the concave convex, the mold releasability of a transparent membrane 2861 and the press plate 2901 becomes good, and manufacture effectiveness improves. In addition, temperature management is also important for the press plate 2901 and a transparent material 2861. As for the press plate 2901, it is more desirable than a transparent membrane 2861 to make temperature low about 15 degrees from 5 times. In addition, as for mold releasability etc., the direction made relation with reverse temperature depending on the class of transparent membrane 2861 may become good. Therefore, it is necessary to fully experiment and to define conditions.

[0122] Moreover, that to which olefin system resin films, such as a silicon resin film, a

fluororesin film, polyethylene, and polypropylene, were illustrated as a ** form film, and spreading etc. made silicon resin and a fluororesin the front face of a resin film is illustrated. If others penetrate ultraviolet rays and have a certain amount of flexibility, they are good anything. For example, a glass substrate etc. can be used.

[0123] Moreover, after removing the press plate 2901 so that it may illustrate by 290 (d), UV (light) is irradiated at the transparent membrane 2861 whole, and a non-hardened resinous principle is stiffened completely. Also in a heat-curing type case, this has the same transparent membrane 2861.

[0124] In addition, although [the manufacture approach explained in drawing 286, drawing 290, etc. / a transparent membrane 2861] an ultraviolet curing type is used, this invention is not limited to this. For example, it cannot be overemphasized that resin ingredients, such as a room-temperature-setting type of 2 liquid type which it begins to harden by mixing a thermoplastic type resin ingredient, a heat-curing type resin ingredient, and 2 liquid, etc. can be used. In the above case, a polymer 2861 does not need to be a transparent material. The selection range of the polymer ingredient 2861 can also use breadth, epoxy system resin, phenol system resin, etc. In this case, after forming irregularity 2863, heating, neglect, etc. are carried out and a flection 2802 is formed. Of course, the press plate 2901 may be stiffened in the condition of having pushed against the transparent membrane 2861. Moreover, the reflective film etc. is formed in the required part of a flection 2802. About the configuration of the reflective film, since drawing 280 explained, it omits.

[0125] Drawing 287 is other examples of this invention. Up to drawing 287 (a), since it is the same as that of other examples, explanation is omitted.

[0126] In drawing 287 (b), heights 2871 are formed on the closure film 73. It is made in agreement [the formation location of heights 2871] with a flection 2802 formation location. That is, it is the periphery of a pixel periphery or the light-emitting part of a pixel. By the liquid crystal display panel, it is the formation location of a black matrix (BM). Heights 2871 are formed using inorganic materials, such as SiO2 and SiNx. Moreover, an organic material may be used like a transparent membrane 2861. As the formation approach of heights 2871, an inorganic thin film or an organic thin film is vapor-deposited or applied by the thickness of 0.5-3 micrometers on the closure film 73 or a closure plate. A mask is formed on it and it etches with a negative or a positive using said mask (drawing 287 (b)).

[0127] Next, a transparent membrane 2861 is applied to the whole viewing area 21 so that it may illustrate to drawing 287 (c). In addition, spreading may use which approaches (technique), such as offset printing, screen-stencil, spreading with a roller, and spreading with a spinner.

[0128] As for the resin to apply, it is desirable to set viscosity to 5 or more cp 40 or less cp. That is, that which fell viscosity comparatively is used. A transparent membrane 2861 is smoothly formed along with heights 2871. As mentioned above, in drawing 287, a flection 2802 is formed by heights 287 and the transparent membrane 2861. Moreover, the reflective film etc. is formed in the required part of a flection 2802. About the configuration of the reflective film, since drawing 280 explained, it omits.

[0129] In addition, in drawing 287 (c), although a transparent membrane is applied to the whole viewing area 21, it may not limit to this, and the thin film which consists of an inorganic material may be vapor-deposited. By vapor-depositing an inorganic material, a flection 2802 is formed of the irregularity of heights 2871.

[0130] Drawing 288 is other examples of this invention. Up to drawing 288 (a), since it is the same as that of other examples, explanation is omitted. In drawing 288 (b), the metal mask 2881 is arranged on the closure film 73 or a closure lid. The closure film 73 side has large opening, and, on the other hand, as for opening of the metal mask 2881, the side is narrow.

[0131] In addition, the metal mask 2881 is produced with the magnetic substance, and

adsorbs the metal mask 2881 magnetically with a magnet from the rear face of a substrate 49. By magnetism, the metal mask 2881 is stuck without a substrate and a clearance.

[0132] In order to carry out the metal mask 2881 explained in drawing 288 as [touch / the closure film 73 / directly] (or contacting the closure film 73 as much as possible, and twisting like), it forms a projection with a height of 1.5-3 micrometers in the rear face of the metal mask 2881. Or a projection with a height of 1.5-3 micrometers is formed in the front face of the closure film 73 or a closure lid. This projection forms the EL film 47 in the part which does not carry out vacuum evaporationo etc. For example, it is between the pixels which adjoined.

[0133] Inorganic materials, such as SiO2 and SiNx, are made to deposit through the metal mask 2881 so that it may illustrate in drawing 288 (b). A deposition part is a formation part of a flection 2802. Moreover, an organic material may be used like a transparent membrane 2861 instead of an inorganic material. A flection 2802 can be formed using the metal mask 2881 as mentioned above.

[0134] Drawing 280 was the flections (or light reflex section) 2802, such as the shape of prism. However, this invention is not limited to this. For example, corresponding to a pixel 16, the micro-lens-like flection 2802 may be formed so that it may illustrate to drawing 289. As for a micro lens, it is desirable to make it the letter of a sign curve. Moreover, although forming in the shape of radii is desirable, it may not limit to this and you may be boiled fish paste-like. As for the height of a micro lens, it is desirable to be referred to as 15 micrometers or more 3100 micrometers or less.

[0135] Ti is vapor-deposited to the soda glass substrate which becomes the basis of a micro-lens substrate, and the circular aperture corresponding to a pixel is opened by photograph ring RAFI. Next, it dips in the melting liquid of the nitrate of univalent ion, and heat-treats at 400 degrees or more. At the time of heating, the cation under melting carries out isotropic diffusion into a glass substrate from an opening aperture, and the ion exchange is performed. If the ion exchange is carried out, the part will produce refractive-index distribution. Refractive indexes are 1.5-1.7. A micro lens is produced as mentioned above.

[0136] Moreover, a micro lens is formed with the La Stampa technique. This La Stampa technique applies the method which OMRON Corp. has adopted as the approach of micro-lens formation, the method which Matsushita Electric uses as a formation method of a microlens with the pickup lens of CD. Moreover, the flection 2802 of drawing 289 can also be formed by the diffraction grating. Since other matters are the same in drawing 280, explanation is omitted.

[0137] With the configuration of drawing 280, the refraction sheet is attached on the closure film 73 (it arranged or forms). The refraction section 2801 is formed on a triangle, a polygon, or radii so that the refraction sheet 2801 may correspond to a pixel 16. That is, although [the refraction section 2801] it is concave convex, this invention is not limited to this. For example, a crevice may be filled up with refraction ingredient 2802b so that it may illustrate to drawing 362 (formation). Or heights may be filled up with refraction ingredient 2802a (formation).

[0138] Refraction section 2802a is formed with a high refractive-index ingredient (restoration), and refraction section 2802b is formed with a low refractive-index ingredient (restoration). Or refraction section 2802a may be formed with a low refractive-index ingredient (restoration), and refraction section 2802b may be formed with a high refractive-index ingredient (restoration). A plantar-flexion chip box ingredient chooses 2 magnesium flux, diacid-ized silicon, 3 aluminum oxides, a 2 fluoridation cerium, or silicon monoxide. A high refraction ingredient chooses 3 oxidization 2 yttrium, a zirconium dioxide, a diacid-ized hafnium, 5 oxidization 2 tantalum, a cerium dioxide, a titanium dioxide, zinc sulfide, or ITO and IZO.

[0139] An organic material is sufficient although the above is an inorganic material. For example, the acrylic resin of a fluorine system is illustrated as a plantar-flexion chip box ingredient. In addition, a liquid or gel can also be used. A refractive index is illustrated for gels, such as purity, silicon, and ethylene glycol, ethyl alcohol, methyl alcohol, etc. as 1.50 or less or more 1.3 low refractive-index ingredient, and liquids, such as salicylic acid methyl, are illustrated as a comparatively high refractive-index ingredient. The refraction sheet 2801 is constituted by being filled up with these etc.

[0140] If the refraction sheet 2801 is formed as shown in drawing 362, it will become a plane on a sheet 2801 and will become easy to stick a polarizing plate etc. on this flat surface. Moreover, it can perform easily coating a front face with UV resin beyond 6H etc. Therefore, the front face of a sheet 2801 can be protected. In addition, the upper and lower sides of the refraction sheet 2801 may be attached upside down so that it may illustrate to drawing 363. Thus, if constituted, it can prevent that refraction section 2802a gets damaged mechanically. In addition, 73 may not function as closure film but may be operated as a protection sheet (protective coat).

[0141] Moreover, it is the same also in the example of drawing 289. The heights of refraction section 2802a may be filled up with refraction ingredient 2802b so that it may illustrate to drawing 364 (formation). Or the crevice of refraction section 2802b may be filled up with refraction ingredient 2802a (formation).

[0142] Moreover, like drawing 363, the upper and lower sides of the refraction sheet 2801 may be attached upside down so that it may illustrate to drawing 365. Thus, if constituted, it can prevent that refraction section 2802a gets damaged mechanically. In addition, 73 may not function as closure film but may be operated as a protection sheet (protective coat).

[0143] A vacuum evaporation system uses the equipment which converted commercial high vacuum vacuum evaporationo equipment (the Japan vacuum-technology incorporated company make, EBV-6DA mold). A main exhauster is the turbo molecular pump (the Osaka vacuum incorporated company make, TC1500) of 1500l. of exhaust velocity, and min, a ultimate vacuum is less than [abbreviation 1x10e-6Torr], and all vacuum evaporationo is performed in the range of 2 - 3x10e-6Torr. Moreover, all vacuum evaporationo is good to carry out by connecting DC power supply (Kikusui electronic incorporated company make, PAK10-70A) to the resistance heating type vacuum evaporationo boat made from a tungsten.

[0144] Thus, on the array substrate arranged in a vacuum layer, 20-50nm of carbon film is formed. Next, a 4-(N and N-bis(p-methylphenyl) amino)-alpha-phenyl stilbene is formed in about 5nm of thickness with the evaporation rate of 0.3 nm/sec as a hole injection layer.

[0145] As an electron hole transportation layer, vapor codeposition of N, N'-bis(4'-diphenylamino-4-biphenylyl)-N, an N'-diphenyl benzidine (the Hodogaya chemistry incorporated company make), and the 4-N and N-diphenylamino-alpha-phenyl stilbene was carried out with the evaporation rate of 0.3 nm/s and 0.01 nm/s, respectively, and they were formed in about 80nm of thickness. tris (8-quinolinolato) aluminum (said -- Renhua -- study incorporated company make) is formed in about 40nm of thickness with the evaporation rate of 0.3 nm/sec as a luminous layer (electron transport layer).

[0146] next -- as an electron injection electrode -- an AlLi alloy (high grade chemistry incorporated company make --) Only Li is formed in about 1nm of thickness with the evaporation rate of about 0.1 nm/sec at low temperature from the aluminum/Li weight ratios 99/1. Then, the temperature up of the AlLi alloy was carried out further, and from the condition in which Li was all out, only aluminum was formed in about 100nm of thickness with the evaporation rate of about 1.5 nm/s, and was used as the electron injection electrode of a laminating mold.

[0147] Thus, after the created organic thin film EL element leaked the inside of a vacuum evaporationo tub with desiccation nitrogen, under desiccation nitrogen-gas-atmosphere mind,

it stuck the Corning 7059 glass closure free wheel plate 41 with the seal adhesives (sealing compound) 45 (the product made from Anelva, Inc., trade name super back seal 953-7000), and was taken as the display panel. In addition, a drying agent 55 is arranged in the space of the closure free wheel plate 41 and the array substrate 49. This is because the organic electroluminescence film is weak to humidity. The moisture which permeates a sealing compound 45 with a drying agent 55 is absorbed, and degradation of the organic electroluminescence film 47 is prevented.

[0148] In order to control osmosis of the moisture from a sealing compound 45, it is a good cure to lengthen the path (pass) from the outside. For this reason, the detailed irregularity 43 and 44 is formed in the periphery of a viewing area in the display panel of this invention. The heights 44 formed in the periphery of the array substrate 49 are formed in a duplex at least. As for spacing (formation pitch) of a convex and a convex, it is desirable to form in 100 micrometers or more 500 micrometers or less, and, as for the height of a convex, it is desirable to be referred to as 30 micrometers or more 300 micrometers or less. These heights are formed with the La Stampa technique. This La Stampa technique applies the method which OMRON Corp. has adopted as the approach of micro-lens formation, the method which Matsushita Electric uses as a formation method of a microlens with the pickup lens of CD.

[0149] On the other hand, heights 43 are formed also in the closure free wheel plate 41. The formation pitch of heights 43 is made the same as that of the formation pitch of heights 44. Thus, heights 44 fit into heights 43 exactly by making the same a formation pitch with heights 43 and 44. Therefore, the location gap with the closure free wheel plate 41 and the array substrate 49 does not occur at the time of manufacture of a display panel. A sealing compound 45 is arranged between heights 43 and 44. A sealing compound 45 prevents permeation of the moisture from the outside while pasting up the closure free wheel plate 41 and the array substrate 49.

[0150] It is desirable to use what consists of resin acrylic in UV (ultraviolet rays) hardening mold as a sealing compound 45. Moreover, as for acrylic resin, it is desirable to use what has a fluorine radical. In addition, the adhesives or the binder of an epoxy system may be used. As for the refractive index of adhesives or a binder, it is desirable to use or more 1.47 1.54 or less thing. As for especially seal adhesives, it is desirable to add impalpable powder, such as impalpable powder of titanium oxide and silicon oxide, at 95% or less of a rate 65% or more by the weight ratio. Moreover, as for the particle diameter of this impalpable powder, it is desirable to consider as 20-micrometer or more average diameter of 100 micrometers or less. The effectiveness which controls penetration of the humidity from the forge-fire outside where the weight ratio of impalpable powder increases becomes high. However, if many [too], air bubbles etc. will tend to enter, space will become large on the contrary, and the seal effectiveness will fall.

[0151] As for the weight of a drying agent, it is desirable to carry out 0.04g or more per die length of 10mm of seal 0.2g or less. It is desirable to carry out 0.06g or more per die length of 10mm of seal 0.15g or less especially. The amount of a drying agent becomes empty, shortly after there is too nothing, there is little moisture prevention effectiveness and an organic electroluminescence layer deteriorates. If many [too], in case a drying agent will carry out a seal, it cannot become a failure, and a good seal cannot be performed.

[0152] Although it is the configuration closed using the free wheel plate 41 of glass in drawing 4, you may be the closure using a film like drawing 7. For example, using for the film of an electrolytic capacitor what vapor-deposited DLC (diamond- -like carbon) as a closure film is illustrated. This film has very bad moisture permeability (moisture proof). This film is carried out closure film 74, and is used. Moreover, it cannot be overemphasized that the configuration thing which vapor-deposits the DLC film etc. directly on the front face

of an electrode 72 is good. That is, it closes with a thin film. The thickness of a thin film is n-d (n calculates those refractive indexes by making them synthesis (n-d of each thin film being calculated), when the laminating of the refractive index of a thin film and two or more thin films is carried out.). d synthesizes and calculates those refractive indexes, when the laminating of the thickness of a thin film and two or more thin films is carried out. It is good to make it become below the luminescence dominant wavelength lambda of EL element 15. By satisfying this condition, the optical ejection effectiveness from EL element 15 doubles [more than] as compared with the case where it closes with a glass substrate. Moreover, the alloy, mixture, or laminated material of aluminum and silver may be formed.

[0153] Not using a cover 41, the configuration closed by the closure film 74 is called the thin film closure as mentioned above. The thin film closure in the case of the bottom ejection which takes out light from a substrate 49 side forms the aluminum electrode used as a cathode on EL film after forming EL film. Next, the resin layer as a buffer coat is formed on this aluminum film. Organic materials, such as an acrylic and epoxy, are illustrated as a buffer coat. Moreover, as for thickness, 1-micrometer or more thickness of 10 micrometers or less is suitable. As for thickness, 2-micrometer or more thickness of 6 micrometers or less is suitable still more preferably. The closure film 74 on this buffer film is formed. If there is no buffer film, the structure of EL film will collapse with stress and a defect will occur in the shape of a muscle. As the closure film 74 was mentioned above, the layer structure (structure which carried out the multilayer vacuum evaporationo of a dielectric thin film and the aluminum thin film by turns) of DLC (diamond- -like carbon) or an electric-field capacitor is illustrated.

[0154] The thin film closure in the case of ejection when taking out light from EL layer side forms the Ag-Mg film used as a cathode by 20A or more 300A thickness on EL film after forming EL film. Moreover transparent electrodes, such as ITO, are formed and low resistance is formed. Next, the resin layer as a buffer coat is formed on this electrode layer. The closure film 74 is formed on this buffer film.

[0155] It is reflected by the reflective film 46, and the one half of the light generated from the organic electroluminescence layer 47 is penetrated with the array substrate 49, and outgoing radiation is carried out. However, outdoor daylight is reflected, a reflect lump occurs and the reflective film 46 reduces display contrast. For this cure, lambda/4 plate 50 and the polarizing plate 54 are arranged to the array substrate 49. In addition, when a pixel is a reflector, outgoing radiation of the light generated from the EL layer 47 is carried out to above. Therefore, it cannot be overemphasized that a phase plate 50 and a polarizing plate 54 are arranged to an optical outgoing radiation side. In addition, a reflective mold pixel constitutes the pixel electrode 48 from aluminum, chromium, silver, etc., and is obtained. Moreover, an interface with an organic electroluminescence layer becomes large by preparing heights (or concave heights) in the front face of the pixel electrode 48, and luminescence area becomes large, and luminous efficiency improves. In addition, when the reflective film used as a cathode (anode) is formed in a transparent electrode or a reflection factor can be reduced to 30% or less, the circular polarization of light plate is unnecessary. It is because a reflect lump decreases sharply. Moreover, interference of light decreases and is also desirable.

[0156] Moreover, the contrast of an organic EL panel can be improved by negating the outdoor daylight reflection realized by forming a two-layer thin film in the interior of a display by optical interference. Cost can be reduced compared with the case where the conventional circular polarization of light plate is used. Moreover, the problem of the diffuse reflection which the circular polarization of light plate was holding, and the problem of the angle-of-visibility dependency of a foreground color and the thickness dependency of an organic electroluminescence luminous layer are solvable.

[0157] Between a substrate 49 and a polarizing plate (polarization film) 54, one sheet or two

or more phase films (a phase plate, a phase rotation means, a phase contrast plate, phase contrast film) are arranged. It is desirable to use a polycarbonate as a phase film. A phase film makes outgoing radiation light generate phase contrast for incident light, and is contributed to performing light modulation efficiently.

[0158] In addition, an organic resin plate or organic resin films, such as polyester resin, PVA resin, polysulphone resin, vinylchloride resin, ZEONEX resin, acrylic resin, and polystyrene resin, etc. may be used as a phase film. In addition, the crystal of Xtal etc. may be used. As for the phase contrast of one phase plate, it is desirable to be referred to as 50nm or more 350nm or less at 1 shaft orientations, and it is desirable to be referred to as 80 morenm or more 220nm or less.

[0159] In addition, it cannot be overemphasized that the circular polarization of light plate 74 (circular polarization of light film) which unified the phase film and the polarizing plate so that it might illustrate to drawing 7 may be used.

[0160] As for the phase film 50, it is desirable for a color or a pigment to color and to give the function as a filter. The red (R) purity of especially organic electroluminescence is bad. Therefore, the fixed wavelength range is cut with the colored phase film 50, and a color temperature is adjusted. As for a color filter, it is common to be prepared by pigment-content powder type resin as a dyeing filter. A pigment absorbs the light of a specific wavelength band and penetrates the light of the wavelength band which was not absorbed.

[0161] A part or the whole of a phase film may be colored as mentioned above, or a diffusion function may be given to a part or the whole. Moreover, embossing of the front face may be carried out, or an antireflection film may be formed for acid resisting. Moreover, it is desirable to form a light-shielding film or the light absorption film in a part without the part or trouble which is not effective in image display, and to demonstrate the improvement effectiveness in contrast according to antihalation in to tighten the black level of a display image ****. Moreover, a micro lens may be formed the shape of boiled fish paste, and in the shape of a matrix by forming irregularity in the front face of a phase film. A micro lens is arranged so that it may correspond to one pixel electrode or a pixel in three primary colors, respectively.

[0162] Although described also in advance, the function of a phase film may be given to a color filter. For example, phase contrast can be generated, when rolling out at the time of formation of a color filter or making it phase contrast arise in the fixed direction according to photopolymerization. In addition, phase contrast may be given by carrying out photopolymerization of the smoothing film 71 of drawing 7. Thus, if constituted, it becomes unnecessary not to constitute a phase film or to arrange it out of a substrate, the configuration of a display panel becomes simple, and low cost-ization can be desired. In addition, it cannot be overemphasized that the above matter may be applied to a polarizing plate.

[0163] As a main ingredient which constitutes a polarizing plate (polarization film) 54, a TAC film (triacetyl cellulose film) is the optimal. A TAC film is because it has the outstanding optical property, surface smooth nature, and processing suitability. About manufacture of a TAC film, it is optimal to produce with a solution flow casting film production technique.

[0164] The thing of the resin film with which the polarizing plate added iodine etc. to poly vinyl alcohol (PVA) resin is illustrated. Since the polarizing plate of the polarization separation means of a pair performs polarization separation by absorbing the polarization component of a different direction from specific polarization shaft orientations among incident light, its use effectiveness of light is comparatively bad. Then, the reflective polarizer which performs polarization separation may be used by reflecting the polarization component (reflective polarizer: RIFUREKUTIBU polarizer) of a different direction from specific polarization shaft orientations among incident light. Thus, if constituted, the use

effectiveness of light will increase with a reflective polarizer, and a display brighter than the above-mentioned example using a polarizing plate will be attained.

[0165] Moreover, as a polarization separation means of this invention, it is also possible besides such a polarizing plate or a reflective polarizer to use what combined the cholesteric-liquid-crystal layer and lambda (1/4) plate, for example, the thing divided into reflective polarization and transparency polarization using Brewster's include angle, the thing using a hologram, a polarization beam splitter (PBS), etc.

[0166] The AIR coat is given to the front face of a polarizing plate 54 although not illustrated in drawing 4. The configuration which forms an AIR coat by dielectric monolayer or multilayers is illustrated. In addition, the resin of a low refractive index of 1.35-1.45 may be applied. For example, the acrylic resin of a fluorine system etc. is illustrated. Or more 1.37 1.42 or less thing of a refractive index is [especially a property] good.

[0167] Moreover, an AIR coat has the configuration of three layers, or a two-layer configuration. In addition, in the case of three layers, it is used in order to prevent reflection in the wavelength band of the large light, and it calls this a multi-coat. In a two-layer case, it is used in order to prevent reflection in the wavelength band of the specific light, and it calls this V quart. A multi-coat and V quart are properly used according to the application of a display panel. In addition, not the thing to limit more than two-layer but one layer is sufficient.

[0168] In the case of a multi-coat, optical thickness carries out $nd1=lambda/4$ laminatings of $nd1=lambda/2$ and the magnesium fluoride (MgF2) for $nd=lambda/4$, and a zirconium (ZrO2), and an aluminum oxide (aluminum 2O3) is formed. Usually, a thin film is formed as a value of 520nm or near of those as lambda. optical in silicon monoxide (SiO) in the case of V quart -- thickness $nd1=lambda/4$, and magnesium fluoride (MgF2) -- $nd1=lambda/4$ or yttrium oxide (Y2O3), and magnesium fluoride (MgF2) -- $n d1=lambda/4$ laminatings are carried out, and it forms. It is better to use Y2O3, when modulating blue glow, since SiO has an absorption band region in a blue side. Moreover, since the direction of Y2O3 is stable also from the stability of the matter, it is desirable. Moreover, SiO2 thin film may be used. Of course, it is good also as an AIR coat using the resin of a low refractive index etc. For example, acrylic resin, such as a fluorine, is illustrated. As for these, it is desirable to use an ultraviolet curing type.

[0169] In addition, in order to prevent that static electricity is charged by the display panel, it is desirable to apply the resin of a hydrophilic property to front faces, such as a display panel. In addition, in order to prevent surface reflection, embossing may be performed on the front face of a polarizing plate 54 etc.

[0170] Moreover, although TFT is connected to the pixel electrode 48, it is not limited to this. It cannot be overemphasized that a diode method (TFD) besides a thin film transistor (TFT), a varistor, a thyristor, ring diode, phot DAODO, a photo transistor, FET, an MOS transistor, a PLZT component, etc. are sufficient as an active matrix as a switching element. That is, a switching device 11, a driver element 11, and the thing to constitute can use these either.

[0171] Moreover, as for TFT, it is desirable to adopt LDD (low doping drain) structure. In addition, all the general component that carry out transistor actuation of switching, such as FET, etc. is meant in TFT. Moreover, it cannot be overemphasized that the configuration of EL film, panel structure, etc. are applicable also to a simple matrix type display panel. Moreover, it cannot be overemphasized that it does not limit to this although an example raises an organic EL device (OEL, PEL, PLED, OLED) 15 and this specification explains it as an EL element, and it is applied also to an inorganic EL element.

[0172] First, the active-matrix method used for an organic electroluminescence display panel should choose the pixel of 1. specification, and gives required display information. Two conditions that a current can be passed to an EL element through a 2 or 1-frame period must

be satisfied.

[0173] In order to satisfy these two conditions, with the component configuration of the conventional organic electroluminescence shown in drawing 12, the transistor for switching for 1st TFT11a to choose a pixel and 2nd TFT11b are taken as the transistor for a drive for supplying a current to EL element (EL film) 15.

[0174] Although transistor 11a for switching is required for liquid crystal as compared with the active-matrix method used for liquid crystal here, transistor 11b for a drive is required in order to make EL element 15 turn on. Although this reason can hold an ON state by impressing an electrical potential difference in the case of liquid crystal, it is because in the case of EL element 15 the lighting condition of a pixel 16 is unmaintainable if it does not continue passing a current.

[0175] Therefore, in order to continue passing a current, making transistor 11b have to turn on in EL display panel must be continued. First, if both the scanning line and the data line are turned on, a charge will be accumulated in a capacitor 19 through transistor 11a for switching. In order that this capacitor 19 may continue applying an electrical potential difference to the gate of transistor 11b for a drive, even if transistor 11a for switching becomes off, a current continues flowing from the current supply source line 20, and a pixel 16 can be turned on over an one-frame period.

[0176] When displaying gradation using this configuration, it is necessary to impress the electrical potential difference according to gradation as gate voltage of transistor 11b for a drive. Therefore, dispersion in the ON state current of transistor 11b for a drive appears in a display as it is.

[0177] If the ON state current of a transistor is the transistor formed with the single crystal, it is very uniform, but in low-temperature polycrystal galvanized iron JISUTA which the formation temperature which can be formed in a cheap glass substrate formed with the low-temperature polysilicon technique of 450 or less degrees, since dispersion in the threshold has dispersion in the range which is **0.2V-0.5V, corresponding to this, nonuniformity occurs [the ON state current which flows transistor 11b for a drive] in dispersion and a display. Such nonuniformity generates not only dispersion in a threshold electrical potential difference but the mobility of TFT and the thickness of gate dielectric film. Moreover, a property changes also with degradation of TFT11.

[0178] Therefore, in order to obtain a uniform display, it is necessary to control the property of a device by the approach of displaying gradation in analog, strictly, and cannot be satisfied with it of the spec. which is less than the predetermined range about this variation of stopping, in the present low-temperature polycrystal poly-Si TFT. Since this problem is solved, four transistors are prepared in 1 pixel and how to make dispersion in a threshold electrical potential difference compensate by the capacitor, and to acquire a uniform current, the method of forming a current regulator circuit for every pixel, and attaining equalization of a current, etc. can be considered.

[0179] However, since the current by which these approaches are programmed is programmed through EL element 15, when a current path changes, the transistor which controls a drive current to the switching transistor connected to power-source Rhine serves as a source follower, and a drive margin becomes narrow. Therefore, it has the technical problem that driver voltage becomes high.

[0180] Moreover, it is necessary to use the switching transistor linked to a power source in the field where an impedance is low, and the technical problem that it is influenced by property fluctuation of EL element 15 also has this operating range. moreover, when a kink current occurs in the volt ampere characteristic in a saturation region and fluctuation of the threshold electrical potential difference of a transistor occurs in it, if the memorized current value is changed to it, it will obtain to it, and a technical problem is also in it.

[0181] Even if the transistor 11 which controls the current which flows to EL element 15 does not serve as a source follower configuration to the above-mentioned technical problem and the EL element structure of this invention has a kink current in the transistor, it is the configuration which can make small fluctuation of the current value which can suppress the effect of a kink current to min, and is memorized.

[0182] The EL element structure of this invention is specifically formed of two or more transistors 11 and EL elements which a unit pixel becomes from at least four as shown in drawing 1 (a). In addition, a pixel electrode is constituted so that it may lap with a source signal line. That is, the flattening film which consists of an insulator layer or an acrylic ingredient is formed on the source signal line 18, it insulates, and a pixel electrode is formed on this insulator layer. Thus, the configuration which piles up a pixel electrode is called high aperture (HA) structure on the source signal line 18.

[0183] It lets the 1st transistor (TFT or switching element) 11a and 3rd transistor (TFT or switching element) 11c pass by activating 1st gate signal line (the 1st scanning line) 17a (ON electrical potential difference being impressed). between a sink, and the gate of the 1st transistor and a drain is short-circuited for the current value which should be passed to said EL element 15 -- as -- 2nd transistor 11b -- 1st gate signal line 17a, while opening being active (ON electrical potential difference being impressed) and by becoming It is remembered that the gate voltage (or drain electrical potential difference) of 1st transistor 11a passes said current value to the capacitor (a capacitor, storage capacitance) 19 connected between the gate of 1st transistor 11a, and the source.

[0184] In addition, as for the capacity 19 between the source-gates of 1st transistor 11a (capacitor), it is desirable to consider as the capacity of 0.2pF or more. As other configurations, the configuration which forms a capacitor 19 is also illustrated separately. That is, it is the configuration which forms storage capacitance from a capacitor electrode layer, gate dielectric film, and gate metal. It is more desirable to constitute a capacitor from a viewpoint for stabilizing the viewpoint and display action which prevent the brightness fall by leak of M3 transistor 11c separately in this way. In addition, the magnitude of a capacitor (storage capacitance) 19 is good to be referred to as 0.2pF or more 2pF or less, and the magnitude of a capacitor (storage capacitance) 19 is good to be referred to as 0.4pF or more 1.2pF or less especially.

[0185] In addition, for a capacitor 19, it is this better ** to form in the non-display field between the adjoining pixels in general. Generally, when creating full color organic electroluminescence, in order to form an organic electroluminescence layer by the mask vacuum evaporationo with a metal mask, the formation location of EL layer by mask location gap occurs. When a location gap occurs, there is a danger that the organic electroluminescence layer of each color will lap. Therefore, 10micro or more of non-display fields between the pixels which each color adjoins must be left. This part turns into a part which does not contribute to luminescence. Therefore, it becomes an effective means for the improvement in a numerical aperture to form storage capacitance 19 in this field.

[0186] In addition, the metal mask 2881 is produced with the magnetic substance, and adsorbs the metal mask 2881 magnetically with a magnet from the rear face of a substrate 49. By magnetism, the metal mask 2881 is stuck without a substrate and a clearance. The matter about the above manufacture approach is applied to other manufacture approaches of this invention.

[0187] Next, it operates so that 1st gate signal line 17a is passed for it to be inactive (an OFF electrical potential difference is impressed), 2nd gate signal line 17b may be activated, it may change to the path containing the 4th transistor 11d by which the path for which a current flows was connected to said 1st transistor 11a list at EL element 15, and said EL element 15 and the memorized current may be passed to said EL element 15.

[0188] This circuit has four transistors 11 in 1 pixel, and the gate of the 1st transistor M1 is connected to the source of the 2nd transistor M2. The gate of the 2nd transistor and the 3rd transistor M2 is connected to 1st gate signal line 17a, the drain of M2 is connected to the source of M3, and the source of the 4th transistor M4, and the drain of M3 is connected to the source signal line 18. The gate of a transistor M4 is connected to 2nd gate signal line 17b, and the drain of a transistor M4 is connected to the anode electrode of EL element 15.

[0189] In addition, at drawing 1, all TFTF(s) consist of P channels. Although P channels have somewhat low mobility as compared with TFT of N channel, since pressure-proofing cannot generate degradation easily greatly again, either, it is desirable. However, it does not limit only to this invention constituting an EL element configuration from P channels. You may constitute only from an N channel (see drawing 42, drawing 43, drawing 67, etc.). Moreover, you may constitute using both N channel and P channels.

[0190] In addition, the 3rd and 4th transistors are constituted from same polarity, and it constitutes from an N channel, and, as for the 1st and 2nd transistors, constituting from P channels is desirable. Generally a P channel transistor has the large effectiveness which uses 1st transistor 11a as P channels to the EL element which obtains the luminescence reinforcement made into the purpose by there being the features, like there are few reliable kink currents, and controlling a current as compared with N channel transistor.

[0191] Following The EL element configuration of this invention is explained using drawing 13. The EL element configuration of this invention is controlled by two timing. The 1st timing is timing which makes a required current value memorize. When TFT11b and TFT11c turn on to this timing, it becomes drawing 13 (a) as an equal circuit. Here, the predetermined current I1 is written in from a signal line. Thereby, TFT11a will be in the condition that the gate and a drain were connected, and a current I1 will flow through this TFT11a and TFT11c. Therefore, the electrical potential difference of the GETO source of TFT11a turns into the electrical potential difference V1 on which I1 flows.

[0192] TFT11a and TFT11c close the 2nd timing, it is the timing which TFT11d opens and the equal circuit at that time serves as drawing 13 (b). The electrical potential difference V1 between the source-gates of TFT11a becomes [being held with as, and]. In this case, transistor 11a of M1 becomes fixed [the current of I1] in order to always operate in a saturation region.

[0193] In addition, the gate of transistor 11a and the gate of transistor 11c are connected to the same gate signal line 11a. However, the gate of transistor 11a and the gate of transistor 11c may be connected to a different gate signal line 11 (it enables it to control SA1 and SA2 according to an individual). That is, a 1-pixel gate signal line becomes three (the configuration of drawing 1 is two). By controlling the ON/OFF timing of the gate of transistor 11a, and the ON/OFF timing of the gate of transistor 11c according to an individual, the current value variation of EL element 15 by dispersion in a transistor 11 can be reduced further.

[0194] If 1st gate signal line 17a and 2nd gate signal line 17b are carried out in common and it is the conductivity type (N channel and P channels) with which the 3rd and 4th transistors differed, simplification of a drive circuit and the numerical aperture of a pixel can be raised.

[0195] Thus, if constituted, as timing of this invention of operation, the write-in path from a signal line will become off. That is, in case a predetermined current is memorized, if the path for which a current flows has branching, an exact current value will not be memorized by the capacity between the source-gates of M1 (capacitor). By making TFTM3 and TFTM4 into a different electric conduction form, after M3 surely turns off to the timing from which the scanning line changes by controlling each other threshold, it enables M4 to turn on.

[0196] However, since it is necessary to control each other threshold correctly in this case, cautions of a process are required. In addition, although the circuit described above is

realizable with at least four transistors, even if it carries out cascade connection of the transistor 11e (M5) for Miller effect reduction as shown in drawing 1 (b) and the total of a transistor becomes four or more so that more exact timing may control or mention later, the principle of operation is the same. Thus, by considering as the configuration which added transistor 11e, the current programmed through the transistor M3 can pass now with a more sufficient precision to EL element 15.

[0197] In the configuration of drawing 1, it is still more desirable that the current value Ids in the saturation region of 1st transistor 11a satisfies the conditions of a bottom type. In addition, in a bottom type, the value of lambda satisfies or less 0.06 0.01 or more conditions between the adjoining pixels.

[0198] Ids=k*(Vgs-Vth) 2 (1+ Vds*lambda)

In this invention, although the operating range of transistor 11a is limited to a saturation region, generally, it separates from the transistor characteristics in a saturation region from an ideal property, and they are influenced of the electrical potential difference between sow sault drains. This effectiveness is called Miller effect.

[0199] The case where the shift of the threshold set to each transistor 11a in the adjoining pixel deltaVt occurs is considered. In this case, the current value memorized is the same. deltaL, then abbreviation delta Vxlambda are equivalent to a gap of the current value of EL element 15 by changing the threshold of transistor 11a in the shift of a threshold. Therefore, it turns out that lambda must be below 0.01xx/y noting that y (V) is permitted between the pixels which adjoin the permissible dose of a shift of a threshold, in order to suppress a gap of a current below to x (%).

[0200] This allowed value changes with the brightness of application. If the amount of fluctuation has 2% or more of brightness in the brightness field to 100-cd/m2 to 1000 cd/m2, human being will recognize the changed boundary line. Therefore, it is required for the amount of fluctuation of brightness (the amount of currents) to be less than 2%. When brightness is higher than 100 cd/cm2, the brightness variation of the adjoining pixel becomes 2% or more. When using EL display device of this invention as a display for personal digital assistants, the demand brightness is about [100cds //m] two. When the pixel configuration of drawing 1 was actually made as an experiment and fluctuation of a threshold was measured, the adjoining pixel transistor 11a Set and it turned out that the maximum of fluctuation of a threshold is 0.3V. Therefore, in order to suppress fluctuation of brightness within 2%, lambda must be 0.06 or less. However, it is not necessary to carry out to 0.01 or less. It is because human being cannot recognize change. Moreover, in order to attain the variation in this threshold, it is necessary to enlarge transistor size enough, and it is unreal.

[0201] Moreover, it is desirable to constitute so that the current value Ids in the saturation region of 1st transistor 11a may satisfy a bottom type. In addition, it may be 1% or more 5% or less between the pixels which fluctuation of lambda adjoins.

[0202] Ids=k*(Vgs-Vth) 2 (1+ Vds*lambda)

If lambda of the above-mentioned formula has fluctuation even when fluctuation of a threshold does not exist even if between the adjoining pixels, the current value which flows EL will be changed. In order to suppress fluctuation within **2%, fluctuation of lambda must be suppressed to **5%. however -- however, it is not necessary to make it to 1% or less It is because human being cannot recognize change. Moreover, in order to attain 1% or less, it is necessary to enlarge transistor size fairly, and it is unreal.

[0203] Moreover, according to an experiment, an array prototype, and examination, it is desirable that the channel length of 1st transistor 11a sets to 10 micrometers or more 200 micrometers or less. It is desirable that the channel length of 1st transistor 11a sets to 15 micrometers or more 150 micrometers or less still more preferably. This is considered to be because for electric field to be eased and for the kink effectiveness to be suppressed low

when the channel length L is lengthened, and the grain boundaries included in a channel increase in number.

[0204] Moreover, the transistor 11 which constitutes a pixel is formed by the poly-Si TFT formed by the laser recrystallization approach (laser annealing), and it is desirable that the direction of the channel in all transistors is the same direction to the direction of radiation of laser.

[0205] The purpose of invention of this patent proposes the circuitry to which dispersion in transistor characteristics does not affect a display, and four or more transistors are [therefore] required for it. If the property of four transistors does not gather when these transistor characteristics determine a circuit constant, it is difficult to ask for a suitable circuit constant. To the direction of a major axis of laser radiation, by the case where the direction of a channel is level, and the case of being perpendicular, the threshold and mobility of transistor characteristics differ from each other, and are formed. In addition, extent of dispersion is the same in both cases. Horizontally, if perpendicular, the average of ****** of mobility and a threshold differs. Therefore, the more nearly same one of the direction of a channel of all the transistors that constitute a pixel is desirable.

[0206] Moreover, when Cs and the OFF state current value of 2nd transistor 11b are set to Ioff for the capacity value of storage capacitance 19, it is desirable to satisfy a degree type.

[0207] 3 < -- Cs/Ioff < -- 24 -- it is desirable to satisfy a degree type still more preferably.

[0208] 6 < -- Cs/Ioff < -- By setting the OFF state current of 18 transistor 11b to 5 or less pAs, it is possible to stop the current value change which flows EL to 2% or less. This is because the charge stored between the gate-sources (both ends of a capacitor) in the electrical-potential-difference condition of not writing in cannot be held between 1 fields, when leakage current increases. Therefore, if the capacity for are recording of a capacitor 19 is large, the permissible dose of the OFF state current will also become large. Fluctuation of the current value between contiguity pixels can be suppressed to 2% or less by filling said formula.

[0209] Moreover, it is desirable for the transistor which constitutes an active matrix to be constituted by the p-ch polish recon thin film transistor, and to consider as the multi-gate structure where transistor 11b is more than the dual gate. In order that transistor 11b may act as a switch between the source-drains of transistor 11a, the property that an ON/OFF ratio is high as much as possible is required. The high property of an ON/OFF ratio is realizable by making structure of the gate of transistor 11b into the multi-gate structure beyond dual gate structure.

[0210] Moreover, the transistor which constitutes an active matrix consists of polish recon thin film transistors, and it is desirable to make (channel width W) * (channel length L) or less [54-micrometer] into two. [of each transistor] (Channel width W) * (channel length L) and the variation of transistor characteristics have correlation. The cause of dispersion in transistor characteristics has a large thing resulting from dispersion in the energy by the exposure of laser etc., therefore in order to absorb this, it is desirable. [of the structure which contains many exposure pitches (generally about ten micrometers) of laser by the inside of a channel as much as possible] By making (channel width W) * (channel length L) or less [54-micrometer] into two, there is no dispersion resulting from laser radiation, and the thin film transistor to which the property was equal can be obtained. [of each transistor] In addition, if transistor size becomes small too much, property dispersion by area will occur. Therefore, it is made for (channel width W) * (channel length L) to become two or more [9-micrometer]. [of each transistor] In addition, (channel width W) * (channel length L) has still more preferably desirable 16-micrometer or more 2 thing it is made to become two or less. [of each transistor] [45 micrometer]

[0211] Moreover, things are [making it mobility fluctuation of 1st transistor 11a in the adjoining unit pixel be 20% or less] desirable. When mobility runs short, by the time the

charge capacity of a switching transistor deteriorates and it passes a current value required in time amount, capacity between the gate-sources of M1 cannot be charged. Therefore, dispersion in the brightness between pixels can be made below into ****** by suppressing dispersion in migration within 20%.

[0212] Although the pixel configuration explained the above explanation as a configuration of drawing 1, the above matter is applicable also to the configuration illustrated to drawing 21, drawing 43, drawing 71, and drawing 22. Hereafter, configuration, actuation, etc. are explained about pixel configurations, such as drawing 21.

[0213] When setting up the current passed to EL element 15, the electrical potential difference between the GETO sources which produces the signal current passed to TFT11a in TFT11a as a result of [its] Iw is set to Vgs. Since between the gate drains of TFT11a has connected too hastily by TFT11d at the time of writing, TFT11a operates in a saturation region. Therefore, Iw is given by the following formulas.

[0214]

Iw=mu 1, Cox1, and W1/L1/2(Vgs-Vth1) 2 -- (1)

Here, Cox is the gate capacitance per unit area, and is given by Cox=epsilon 0 and epsilonr/d. In the mobility of a carrier, and W, as for vacuous mobility and epsilonr, channel width and L show channel length, epsilon 0 shows [the threshold and mu whose Vth is TFT] the specific inductive capacity of gate dielectric film, and d is the thickness of gate dielectric film.

[0215] Current level will be controlled by TFT1b by which Idd is connected to EL element 15 and a serial if the current which flows to EL element 15 is set to Idd. In this invention, since the electrical potential difference between the GETO sources is in agreement with Vgs of (1) type, if it assumes that TFT1b operates in a saturation region, the following formulas will be realized.

[0216]

Idrv=mu 2, Cox2, and W2/L2/2(Vgs-Vth2) 2 -- (2)

Generally conditions for the thin film transistor (TFT) of an insulated-gate electric field effect mold to operate in a saturation region are given by the following formulas by making Vds into the electrical potential difference between the drain sources.

[0217]

| Vds|>|Vgs-Vth| -- (3)

Here, since it is approached and formed in the interior of a small pixel, TFT11a and TFT11b are profile mu1=mu2 and Cox1=Cox2, and unless especially creativity is put, they are considered to be Vth1=Vth2. Then, the following formulas are easily drawn from (1) type and (2) types at this time.

[0218]

Idrv/Iw=(W2/L2)/(W1/L1) -- (4)

Although it is common in (1) type and (2) types that the value of mu, Cox, and Vth itself varies for every pixel, every product, and every manufacture lot as for the point which it should be careful of here, since (4) types do not contain these parameters, I hear that it is not dependent on these dispersion, and there is a value of Idrv/Iw.

[0219] If it designs with W1=W2 and L1=L2, Idrv/Iw=1, i.e., Iw and Idrv, will become the same value. That is, it is not based on property dispersion of TFT, but since the drive current Idd which flows to EL element 15 becomes the same as that of the signal current Iw correctly, it can control the luminescence brightness of EL element 15 correctly as a result.

[0220] since [as mentioned above,] Vth1 of TFT11a for conversion and Vth2 of TFT11b for a drive are fundamentally the same -- both TFT(s) -- if the signal level of cut-off level is impressed to the gate which is in the common potential of ** mutually -- TFT11a and TFT11b -- it must be in both non-switch-on -- it comes out. However, Vth2 may become low rather than Vth1 according to factors, such as dispersion in a parameter, also within a pixel in

fact. At this time, since the leakage current of subthreshold level flows to TFT11b for a drive, EL element 15 presents fine luminescence. The contrast of a screen falls by this fine luminescence, and a display property is spoiled.

[0221] Especially in this invention, it is set as the appearance to which the threshold voltage Vth2 of TFT11b for a drive does not become lower than the threshold voltage Vth1 of TFT11a for conversion which corresponds within a pixel. For example, even if it makes gate length L2 of TFT11b longer than the gate length L1 of TFT11a and changes the process parameter of these thin film transistors, it is made for Vth2 not to become lower than Vth1. It is possible for this to control very small current leak. The above matter is applied also to TFT11a of drawing 1, and the relation of TFT11d.

[0222] Transistor TFT11for conversion a to which the signal current flows as shown in drawing 21, Others [b / which controls the drive current which flows to the light emitting device which consists of EL element 15 grade / transistor TFT11for drive], Transistor TFT11for taking in c which connects or intercepts a pixel circuit and data-line data by control of the 1st scanning line scanA (SA), By control of the 2nd scanning line scanB (SB) It consists of capacity C19 for writing in the electrical potential difference between the GETO sources of transistor TFT11d for a switch and TFT11a which short-circuit the gate drain of TFT1111a during a write-in period, and holding after termination, EL element 15 as a light emitting device, etc. Therefore, since gate signal lines are each two pixels, they can apply the configuration of the whole specification of this invention explained by drawing 1 explained above, drawing 2, drawing 3, etc., a function, actuation, etc.

[0223] Although TFT11c constitutes drawing 21 and the transistor of N-channel MOS (NMOS) and others is constituted from a P channel MOS (PMOS), this needs to be an example and does not necessarily need to be this passage. Although the terminal of one of these is connected to the gate of TFT11a and the other-end child is connected to Vdd (power-source potential), the fixed potential of not only Vdd but arbitration is sufficient as capacity C. The cathode (cathode) of EL element 15 is connected to touch-down potential. Therefore, it cannot be overemphasized that the above matter is applied to drawing 1 etc.

[0224] The terminal voltage of EL element 15 changes also with temperature. Usually, it becomes low as it is high and temperature becomes high, when temperature is low. This inclination has the relation of a linear. Therefore, it is desirable to adjust a Vdd electrical potential difference by the outside temperature (temperature which is EL element 15 correctly). A temperature sensor detects an outside temperature, feedback of the Vdd electrical-potential-difference generating section is applied, and a Vdd electrical potential difference is changed. A Vdd electrical potential difference is Centigrade 10-degree C change, and it is desirable to make it change 8% or less 2% or more. It is desirable to consider as 6% or less 3% or more especially.

[0225] In addition, as for Vdd electrical potential differences, such as drawing 1, it is desirable to make it lower than the OFF state voltage of TFT11. Specifically, Vgh (OFF state voltage of the gate) should be made higher than Vdd-0.5(V) at least. When lower than this, off leak of TFT occurs and the shot nonuniformity of laser annealing comes to be conspicuous. Moreover, it should be made lower than Vdd+4(V). If too high, the amount of off leaks will increase conversely. Therefore, in the OFF state voltage (electrical-potential-difference side near [in drawing 1] Vgh, i.e., supply voltage) of the gate, supply voltage (drawing 1 Vdd) should also carry out the twist below +4 (V) more than -0.5 (V). Supply voltage (drawing 1 Vdd) should also make the twist still more desirable below +2 (V) more than 0 (V). That is, it is made for the OFF state voltage of TFT impressed to a gate signal line to become sufficiently off. When TFT is n channels, Vgl serves as OFF state voltage. Therefore, it is made for Vgl to serve as range below 0.5 (V) more than -4 (V) to a GND electrical potential difference. The thing below 0 (V) to do for the range is [more than -2

(V)] still more preferably desirable.

[0226] It cannot be overemphasized that it is not limited to this although the above matter describes the pixel configuration of the current program of drawing 1, and it can apply also to the pixel configuration of electrical-potential-difference programs, such as drawing 54, drawing 67, and drawing 103. In addition, as for Vt offset cancellation of an electrical-potential-difference program, it is desirable to compensate every R, G, and B according to an individual.

[0227] The configuration of drawing 21 is equipped with two or more pixels containing EL element 15 of the current drive mold which emits light in response to supply of a drive current while it is allotted to the intersection of a data-line drive circuit including the current source CS which generates the signal current Iw which has the scanning-line drive circuit which makes sequential selection of the scanning lines scanA and scanB, and the current level according to brightness information, and is serially supplied to data-line data, and each scanning lines scanA and scanB and each data-line data.

[0228] The pixel configuration shown in drawing 21 as a description matter consists of the accession department which incorporates the signal current Iw from the data-line data concerned, a transducer which once changes and holds the current level of the incorporated signal current Iw to a voltage level, and a mechanical component which passes the drive current which has the current level according to the held voltage level to the light emitting device OLED15 (it may otherwise be called EL, OEL, PEL, and PLED for short) concerned, when the scanning line scanA concerned is chosen. Specifically, said accession department consists of transistor TFT11for taking in c.

[0229] Said transducer contains the capacity C connected with thin film transistor TFT11a for conversion equipped with the gate, the source, the drain, and the channel at the gate. The gate is made to generate the voltage level which passed to the channel the signal current Iw incorporated by thin film transistor TFT11for conversion a, and the accession department, and was changed, and the voltage level produced in capacity C19-TO is held.

[0230] Furthermore, said transducer contains thin film transistor TFT11d for a switch inserted between the thin film transistor TFT11a drain for conversion, and the gate. Thin film transistor TFT11d for switching flows, when changing the current level of the signal current Iw into a voltage level, the drain and the gate of thin film transistor TFT11a for conversion are connected electrically, and the gate of TFT11a is made to produce the voltage level on the basis of the source. Moreover, thin film transistor TFT11d for a switch is intercepted when holding a voltage level in capacity C, and it separates the capacity C19 linked to the gate of thin film transistor TFT11a for conversion, and this from the drain of TFT11a.

[0231] Moreover, said mechanical component contains thin film transistor TFT11b for a drive equipped with the gate, a drain, the source, and a channel. The drive current which thin film transistor TFTb for a drive accepts in the gate the voltage level held at capacity C19, and has the current level according to it is passed to EL element 15 through a channel. The gate of thin film transistor TFT11a for conversion and the gate of thin film transistor TFT11b for a drive are connected directly, and he constitutes current Miller circuit, and is trying for the current level of the signal current Iw and the current level of a drive current to serve as proportionality.

[0232] Thin film transistor TFT11b for a drive operates in a saturation region, and passes the drive current according to the difference of the voltage level and threshold voltage which were impressed to the gate to EL element 15.

[0233] Thin film transistor TFT11b for a drive is set as the appearance to which the threshold voltage does not become lower than the threshold voltage of thin film transistor TFT11a for conversion which corresponds within a pixel. Specifically, TFT11b is set as the appearance to which the gate length does not become shorter than the gate length of TFT11A. Or TFT11b

may be set up so that the gate dielectric film may not become thinner than the gate dielectric film of TFT11a which corresponds within a pixel.

[0234] Or TFT11b may adjust the high impurity concentration injected into the channel, and may set it as the appearance to which threshold voltage does not become lower than the threshold voltage of TFT11a which corresponds within a pixel. As for TFT11a and TFT11b, both should be turned off, if the signal level of cut-off level is impressed to the gate of both the thin film transistors by which common connection was made when it sets up temporarily so that the threshold voltage of TFT11a and TFT11b may become the same. However, dispersion in a process parameter is also in a pixel slightly in fact, and the threshold voltage of TFT11b may become low from the threshold voltage of TFT11a.

[0235] At this time, since the feeble current of subthreshold level flows to TFT11b for a drive also with the signal level below cut-off level, EL element 15 fine-emits light and the contrast fall of a screen appears. Then, gate length of TFT11b is made longer than the gate length of TFT11a. Even if it changes the process parameter of a thin film transistor within a pixel, it is made for the threshold voltage of TFT11b not to become lower than the threshold voltage of TFT11a by this.

[0236] In the comparatively short short-channel-effect field A, Vth goes up [gate length L] with the increment in gate length L. On the other hand, in the comparatively big control field B, gate length L is not concerned with gate length L, but Vth's is almost fixed. Gate length of TFT11b is made longer than the gate length of TFT11a using this property. For example, when the gate length of TFT11a is 7 micrometers, gate length of TFT11b is set to about 10 micrometers.

[0237] While the gate length of TFT11a belongs to the short-channel-effect field A, the gate length of TFT11b may be made to belong to the control field B. Thereby, while being able to control the short channel effect in TFT11b, the threshold voltage reduction by fluctuation of a process parameter can be controlled. By the above, the leakage current of the subthreshold level which flows to TFT11b can be controlled, fine luminescence of EL element 15 can be suppressed, and it can contribute to a contrast improvement.

[0238] The drive approach of the pixel circuit shown in drawing 21 is explained briefly. First, at the time of writing, the 1st scanning line scanA and the 2nd scanning line scanB are made into a selection condition. By connecting a current source CS to data-line data, where both the scanning lines are chosen, the signal current Iw according to brightness information flows to TFT11a. A current source CS is a source of a good transformation style controlled according to brightness information. At this time, since it has connected too hastily electrically by TFT11d between the gate drains of TFT11a, (3) types are materialized, and TFT11a operates in a saturation region. Therefore, between the GETO source, the electrical potential difference Vgs given by (1) formula arises.

[0239] Next, scanA and scanB are made into the condition of not choosing. In detail, TFT11d is first made into an off condition by making scanB into a low. Vgs is held by this with capacity C19. Next, since a pixel circuit and data-line data are electrically intercepted by making scanA into a high level and setting to OFF, the writing to another pixel can be performed through data-line data after that. Here, although the data which a current source CS outputs as current level of the signal current need to be effective when scanB is un-choosing, they may be made into the level (for example, write-in data of the following pixel) of arbitration after that.

[0240] Since common connection of TFT11a, the gate, and the source is made [both] and TFT11b is approached and formed in the interior of a small pixel, if TFT11b is operating in the saturation region, the current which flows TFT11b will be given by (2) formulas, and will turn into the drive current Idd which flows to this [15], i.e., an EL element. What is necessary is just to give sufficient power-source potential to Vdd so that (3) types may be

materialized in addition even if it takes into consideration the voltage drop in EL element 15 in order to operate TFT11b in a saturation region.

[0241] In addition, like drawing 1 (b) etc., in order to increase an impedance, it cannot be overemphasized that TFT(s) 11e and 11f may be added so that it may illustrate [purpose] to drawing 22. Thus, a better current drive is realizable by adding TFT(s) 11e and 11f. drawing 1 explains other matters -- it comes out and omits.

[0242] Thus, direct current voltage was impressed to EL display device explained by produced drawing 1, drawing 21, etc., and 10mA /was made to carry out a continuation drive with the fixed current density of 2 cm. EL structure has checked luminescence of the green (luminescence maximum wave length lambdamax=460nm) of 7.0V and 200 cd/cm2. A blue light-emitting part is brightness 100 cd/cm2, the color coordinate of x= 0.129, y= 0.105, and a green light-emitting part was brightness 200 cd/cm2, the color coordinate of x= 0.340, y= 0.625, and a red light-emitting part is brightness 100 cd/cm2, and the color coordinate was acquired for the luminescent color of x= 0.649 and y= 0.338.

[0243] Henceforth, the indicating equipment using drawing 1, drawing 21, drawing 43, drawing 71, drawing 22, etc., a display module, an information display and its drive circuit, the drive approach, etc. are explained.

[0244] In a full color organic electroluminescence display panel, improvement in a numerical aperture becomes an important development technical problem. It is for the use effectiveness of light increasing, if a numerical aperture is raised, and leading to a raise in brightness, or reinforcement. What is necessary is just to make small area of TFT which interrupts the light from an organic electroluminescence layer, in order to raise a numerical aperture. Low-temperature polycrystal Si-TFT has one 10 to 100 times the engine performance of this as compared with an amorphous silicon, and since the serviceability of a current is high, it can make magnitude of TFT very small. Therefore, it is desirable to produce a pixel transistor and a circumference drive circuit with a low-temperature polish recon technique in an organic electroluminescence display panel. Of course, although you may form with an amorphous silicon technique, a pixel numerical aperture will become quite small.

[0245] By forming drive circuits, such as a gate driver 12 or the source driver 14, on a glass substrate 46, the resistance which becomes a problem especially with the organic electroluminescence display panel of a current drive can be lowered. Connection resistance of TCP is lost, and also the outgoing line from an electrode becomes short 2-3mm compared with the case of TCP connection, and wiring resistance becomes small. Furthermore, suppose that there is an advantage whose process for TCP connection is lost that ingredient cost falls.

[0246] Next, EL display panel or EL display of this invention is explained. Drawing 2 is an explanatory view centering on the circuit of EL display. The pixel 16 is arranged or formed in the shape of a matrix. The source driver 14 which outputs the current which performs the current program of each pixel to each pixel 16 is connected. The current Miller circuit corresponding to the number of bits of a video signal in the output stage of the source driver 14 is formed. For example, if it is 64 gradation, 63 current Miller circuits are formed in each source signal line, and it is constituted by choosing the number of such current Miller circuits so that a desired current can be impressed to the source signal line 18.

[0247] In addition, the minimum output current of one current Miller circuit is set to more than 10nA50nA. Especially the minimum output current of current Miller circuit is good to make it more than 15nA35nA. It is for securing the precision of the transistor which constitutes the current Miller circuit in a driver IC 14.

[0248] Moreover, the precharge which emits or charges the charge of the source signal line 18 compulsorily, or a discharge circuit is built in. As for the electrical-potential-difference (current) output value of the precharge which emits or charges the charge of the source signal line 18 compulsorily, or a discharge circuit, it is desirable to constitute so that it can set up

independently by R, G, and B. the threshold of EL element 15 -- RGB -- things -- since -- it is .

[0249] It cannot be overemphasized that the pixel configuration explained above, an array configuration, a panel configuration, etc. are applied to the configuration and approach which are explained below, and equipment. Moreover, it cannot be overemphasized that the pixel configuration which already explained the configuration and approach which are explained below, and equipment, an array configuration, a panel configuration, etc. are applied.

[0250] It is known that an organic EL device has a big temperature dependence property (temperature dependenccy characteristics). In order to adjust the luminescence brightness change by these temperature dependenccy characteristics, nonlinear components, such as a thermistor to which the output current is changed, or posistor, are added to current Miller circuit, and reference current is created in analog by adjusting change by temperature dependenccy characteristics with said thermistor etc.

[0251] In this case, since it is uniquely determined by EL ingredient to choose, a microcomputer etc. does not have to carry out software control in many cases. That is, you may fix to a fixed shift amount etc. with a liquid crystal ingredient. It is important that temperature dependenccy characteristics change with luminescent color ingredients, and it is the point that it is necessary to perform optimal temperature-dependenccy-characteristics compensation to every luminescent color (R, G, B).

[0252] It is necessary to carry out the temperature dependenccy characteristics of each EL element of R, G, and B within fixed limits. It cannot be overemphasized that it is desirable that there is nothing as for the temperature dependenccy characteristics of EL element 15 of R, G, and B. at least -- the temperature-dependenccy-characteristics direction of R, G, and B -- the same direction -- or it is made not to change Moreover, change is change of 10 degrees C of each color Centigrade, and it is desirable to make it change 8% or less 2% or more. It is desirable to consider as 6% or less 3% or more especially.

[0253] Moreover, a microcomputer may perform temperature-dependenccy-characteristics compensation. The temperature of EL display panel is measured with a temperature sensor, and it is made to change with the measured temperature with a microcomputer (not shown) etc. Moreover, you may control to change reference current etc. automatically by microcomputer control etc. at the time of a change, and to be able to display a specific menu display. Moreover, it can constitute so that it can change using a mouse etc. Moreover, you may constitute so that it can change by using the display screen of EL indicating equipment as a touch panel, and displaying a menu, and pressing down a specific part.

[0254] In this invention, a source driver is formed with a semi-conductor silicon chip, and is connected with the terminal of the source signal line 18 of a substrate 46 with the glass technique on chip (COG). As for wiring of signal lines, such as the source signal line 18, metal wiring of chromium, aluminum, silver, etc. is used. It is because wiring of low resistance is obtained by thin wiring width of face. Wiring is the ingredient which constitutes the reflective film of a pixel, when a pixel is a reflective mold, and forming in the reflective film and coincidence is desirable. It is because it can carry out simple [of the process].

[0255] This invention is good also as a configuration which does not limit to a COG technique, loaded the above-mentioned driver IC 14 etc. into the chip-on film (COF) technique, and was connected with the signal line of a display panel. Moreover, Drive IC produces a power source IC 102 separately, and is good also as 3 chip configurations.

[0256] Moreover, a TCF tape may be used. The film for TCF tapes can carry out thermocompression bonding of a polyimide film and the copper (Cu) foil, without using adhesives. In addition to this, there are a method which carries out cast molding of the polyimide which dissolved on Cu foil in piles, and a method which attaches Cu by plating or vacuum evaporationo on the metal membrane which formed by sputtering on the polyimide

film in the film for the TCP tapes which attach Cu to a polyimide film, without using adhesives. Although these any are sufficient, the approach using the TCP tape which attaches Cu to a polyimide film, without using adhesives is the most desirable. It corresponds to the lead pitch of 30 micrometers or less with Cu beam laminate not using adhesives. Since the approach of forming Cu layer by plating or vacuum evaporationo among Cu beam laminates not using adhesives is suitable for thin shape-ization of Cu layer, it is advantageous to detailed-izing of a lead pitch.

[0257] On the other hand, the gate driver circuit 12 is formed with the low-temperature polish recon technique. That is, it forms in the same process as TFT of a pixel. As compared with the source driver 14, internal structure is easy for this and it is because clock frequency is also low. Therefore, even if it forms with a low-temperature polysilicon technique, it can form easily, and narrow picture frame-ization can be realized. Of course, it cannot be overemphasized that a gate driver 12 may be formed with a silicon chip, and you may mount on a substrate 46 using a COG technique etc. Moreover, switching elements, such as Pixel TFT, a gate driver, etc. may be formed with an elevated-temperature polish recon technique, and may be formed with an organic material (organic TFT).

[0258] A gate driver 12 contains shift register 22a for gate signal line 17a, and shift register 22b for gate signal line 17b. Each shift register 22 is controlled by the clock signal (CLKxP, CLKxN) of a non-inverter and a negative phase, and the start pulse (STx). In addition, it is desirable to add the enabling (ENABL) signal which controls the output of a gate signal line and un-outputting, and the up-and-down (UPDWM) signal which carries out the vertical inversion of the shift direction. It is desirable to prepare the output terminal which otherwise checks for a start pulse to be shifted to a shift register, and to be outputted. In addition, the shift timing of a shift register is controlled by the control signal from Control IC (not shown). Moreover, the level shift circuit which performs the level shift of external data is built in. Moreover, an inspection circuit is built in.

[0259] Since the buffer capacity of a shift register 22 is small, the gate signal line 17 cannot be driven directly. Therefore, between the output gates 24 which drive the output and the gate signal line 17 of a shift register 22, at least two or more inverter circuits 23 are formed.

[0260] It is also the same as when forming the source driver 14 directly on a substrate 46 with polysilicon techniques, such as low-temperature polysilicon, and two or more inverter circuits are formed between the gate of analog switches, such as the transfer gate which drives a source signal line, and the shift register of a source driver. The following matters (the output of a shift register and the output stage (matter about the inverter circuit arranged among output stages, such as the output gate or the transfer gate) which drives a signal line are matters common to a source drive and a gate drive circuit.) For example, although it illustrated in drawing 2 as the output of the source driver 14 was connected to the direct source signal line 18, in fact, a multistage inverter circuit is connected and, as for the output of the shift register of a source driver, the output of an inverter is connected to the gate of analog switches, such as the transfer gate.

[0261] An inverter circuit 23 consists of an MOS transistor of P channels, and an MOS transistor of N channel. As explained also in advance, the inverter circuit 23 is connected to the outgoing end of the shift register circuit 22 of the gate driver circuit 12 multistage, and the final output is connected to the output gate 24. In addition, an inverter circuit 23 may consist of only P channels. However, you may constitute not as an inverter but as a mere gate circuit in this case.

[0262] Channel width of TFT of P channels which constitute each inverter circuit 23, or N channel is set to W, channel length is set to L (in on double-gate **, the width of face or the channel length of a channel which constitutes is added), and the degree of the inverter near a 1 and display side is set to N (eye N stage) for the degree of the inverter near a cyst register.

[0263] Multiplex [of the property difference of the inverter 23 connected if there are many connection number of stageses of an inverter circuit 23] (piled up) is carried out, and a difference arises from a shift register 22 in the transfer time to the output gate 24 (time delay variation). For example, in the case of being extreme, the condition of telling that which turns on output gate 24a after 1.0microsec (measuring after a pulse is outputted from a shift register) in drawing 2 (output voltage has changed) that output gate 24b is turned on after 1.5microsec (measuring after a pulse is outputted from a shift register) (output voltage has changed) arises.

[0264] Therefore, although the direction with more than [little / inverter circuit / 23 / which is produced between a shift register 22 and the output gate 24] is good, gate width W of the channel of TFT which constitutes the output gate 24 is very large. Moreover, the gate drive capacity of the output stage of the cyst register 22 is small. Therefore, it is impossible to drive the output gate 24 directly in the gate circuits (NAND circuit etc.) which constitute a shift register. Therefore, although it is necessary to make multistage connection of the inverter, if the ratio of the inverter 23d [of drawing 2] magnitude of W4/L4 (channel width of P channels / channel length of P channels), and W3 of inverter 23c / magnitude of L3 is large, a time delay will become long and variation will also become [the property of an inverter] large, for example.

[0265] The relation between time delay variation (a dotted line shows) and a time delay ratio (a continuous line shows) is shown in drawing 3. (Wn-1/Ln-1) / (Wn/Ln) shows an axis of abscissa. For example, L of inverter 23d and inverter 23c is the same at drawing 2, and if it is 2 W3=W4 (W3 / L3), it is /(W4/L4) =0.5. In the graph of drawing 3, a time delay ratio sets the time of (Wn-1/Ln-1) / (Wn/Ln)=0.5 to 1, and is setting time amount variation as well as delay to 1.

[0266] By drawing 3, it is shown that the time delay to the inverter 23 from an inverter 23 to the next step becomes long, so that it is shown that the connection number of stages of an inverter 23 increases, and time delay variation becomes large, so that (Wn-1/Ln-1) / (Wn/Ln) becomes large, and (Wn-1/Ln-1) / (Wn/Ln) becomes small. It is advantageous on a design to make a time delay ratio and time delay variation less than into two from this graph. Therefore, what is necessary is just to satisfy the conditions of a degree type.

[0267] 0.25 <=(Wn-1/Ln-1)/(Wn/Ln) <=0.75 and the W/L ratio (Wp/Lp) of P channels of each inverter 23, and the W/L ratio (Ws/Ls) of n channels need to satisfy the following relation.

[0268] 0.4 <=(Ws/Ls)/(Wp/Lp) If the number of stages n of the inverter 23 formed between the output gates (or transfer gate) from the outgoing end of a shift register at <=0.8 pan satisfies a degree type, there is also little variation in a time delay and it is good.

[0269] 3 <= n <= A technical problem is in the 8 mobility mu. If mobility mun of a n channel transistor is small, the size of TG and an inverter will become large and power consumption etc. will become large. Moreover, the formation area of a driver becomes large. Therefore, panel size will become large. On the other hand, if large, it will be easy to cause property degradation of a transistor. Therefore, mobility mun has the following good range.

[0270] 50 <= mun <= The slew rate of the clock signal in 150 and a shift register 22 is made below into 500v[/] microsecondec. When a slew rate is high, a n channel deterioration of the transistor is intense.

[0271] In addition, a NAND circuit is sufficient although [drawing 2 / the output of a shift register] an inverter 23 is connected to multistage. It is because an inverter can be constituted also from a NAND circuit. That is, what is necessary is just to consider the connection number of stages of the gate with the connection number of stages of an inverter 23. Relation, such as a W/L ratio explained also in this case until now, is applied. Moreover, the matter explained by the above drawing 2, drawing 3, etc. is applied to drawing 60, drawing 74,

drawing 84, etc.

[0272] Moreover, when the number of the switching transistors of a pixel is P in drawing 2 etc., as for the output from the inverter of the last stage, Vgl is impressed to the gate signal line 17, as for ON state voltage, and, as for OFF state voltage, Vgh is impressed to the gate signal line 17. Conversely, when the switching transistor of a pixel is N channel, as for the output from the inverter of the last stage, Vgl is impressed to the gate signal line 17, as for OFF state voltage, and, as for ON state voltage, Vgh is impressed to the gate signal line 17.

[0273] Although [the above example] a gate driver is produced to a pixel 16 and coincidence with elevated-temperature polish recon or a low-temperature polish recon technique, it does not limit to this. For example, the source driver IC 14 produced with the semiconductor chip and a gate driver IC 12 may be separately loaded into a display panel 82 so that it may illustrate to drawing 26.

[0274] Moreover, when using a display panel 82 for information displays, such as a cellular phone, it is desirable to mount driver ICs 14 and 15 in one side of a display panel, as shown in drawing 26 (the gestalt which mounts a driver IC in one side still in this way is called a three-side free configuration (structure).). Conventionally, the gate driver IC 12 was mounted X side of a viewing area, and the source driver IC 14 was mounted in Y sides. It is because it is easy to design so that the center line of Screen 21 may take the lead in an indicating equipment, and mounting of a driver IC also becomes easy. In addition, a gate driver circuit may be produced with a configuration free three sides with elevated-temperature polish recon or a low-temperature polish recon technique (that is, at least one side is directly formed in a substrate 49 with a polish recon technique among 14 and 12 of drawing 26).

[0275] In addition, with a three-side free configuration, not only the configuration that loaded or formed direct IC in the substrate 49 but the configuration which stuck on one side (or about one side) of a substrate 49 the films (TCP, TAB technique, etc.) which attached ICs 14 and 12 etc. is included. That is, all similar to the configuration, the arrangement, or it by which IC is not mounted or attached in two sides are meant.

[0276] If a gate driver 12 is arranged beside the source driver 14 like drawing 26, the side C meets and it is necessary to form the gate signal line 17 and to form it to the screen-display field 21 (reference, such as drawing 27).

[0277] In addition, the pitch of the gate signal line 17 formed C side is set to 5 micrometers or more 12 micrometers or less. In less than 5 micrometers, a noise will ride on a contiguity gate signal line under the effect of parasitic capacitance. According to the experiment, the effect of parasitic capacitance occurs notably in 7micro or less. In less than 5 more micrometers, image noises, such as the shape of a beat, occur violently in a display screen. It is difficult for especially generating of a noise to differ by right and left of a screen, and to reduce image noises, such as the shape of this beat. Moreover, if 12 micrometers of reduction are exceeded, the frame width of face D of a display panel becomes large too much and is not practical.

[0278] In order to reduce the above-mentioned image noise, it can decrease by arranging the Grant pattern (electric conduction pattern set as the fixed electrical potential difference by a voltage clamp or the potential stabilized as a whole) in the lower layer or the upper layer of a part in which the gate signal line 17 was formed. Moreover, what is necessary is just to arrange the shielding plate (shielding foil (electric conduction pattern set as the fixed electrical potential difference by a voltage clamp or the potential stabilized as a whole)) formed separately on the gate signal line 17.

[0279] Although the gate signal line 17 of C side of drawing 26 may be formed with an ITO electrode, in order to form low resistance, it is desirable to carry out the laminating of ITO and the metal thin film, and to form them. Moreover, forming by the metal membrane is desirable. When carrying out a laminating to ITO, the titanium film is formed on ITO and the

alloy thin film of aluminum or aluminum, and molybdenum is formed on it. Or the chromium film is formed on ITO. In the case of a metal membrane, it forms with an aluminum thin film and a chromium thin film. The above matter is the same in other examples of this invention.

[0280] In addition, in drawing 27 etc., although [wiring 17 etc.] arranged in one side of a viewing area, it may not be limited to this, and it may be arranged to both. For example, gate signal line 17a may be arranged on the right-hand side of a viewing area 21 (formation), and gate signal line 17b may be arranged on the left-hand side of a viewing area 21 (formation). The above matter is the same in other examples.

[0281] In drawing 30, the source driver IC 14 and the gate driver IC 12 are formed into 1 chip (1 chip driver IC14a). If 1 chip is formed, mounting of IC chip to a display panel 82 can be managed with one piece. Therefore, mounting cost can also be reduced. Moreover, the various electrical potential differences used within 1 chip driver IC can also be generated in coincidence.

[0282] In addition, it cannot be overemphasized that the source driver IC 14, a gate driver IC 12, and 1 chip driver IC14a may be produced with semi-conductor wafers, such as silicon, it may not limit to this although mounted in a display panel 82, and you may form in a display panel 82 directly with a low-temperature polish recon technique and an elevated-temperature polish recon technique.

[0283] In drawing 28, although gate drivers 12a and ICs 15b are mounted in the both ends of the source driver IC 14 (or it forms), it is not limiting to this, either. For example, as shown in drawing 26, while adjoined the source driver IC 14 and one gate driver IC 12 may be arranged to a side. In addition, the part illustrated as the thick continuous line in drawing 26 etc. shows the part which the gate signal line 17 arranged in parallel and formed. Therefore, the gate signal line 17 for a number of a scan signal line arranges in parallel the part (bottom of screen) of b, it is formed, and, as for the part (screen upper part) of a, one gate signal line 17 is formed.

[0284] In addition, if two gate drivers 12a and 12b are used like drawing 28, the number of gate signal line 17a which arranges in parallel C side of drawing 28, and is formed will be set to one half of the number of scanning lines (it is because the number of gate signal lines can be arranged every [2 / 1/] to right and left of a screen). Therefore, it cannot be overemphasized that there is the description that a frame becomes equal by right and left of a screen.

[0285] This invention has the description also in the scanning direction of the gate signal line 17, and screen separation. For example, gate driver 12a is connected with gate signal line 17b of the screen upper part in drawing 28. Moreover, gate driver 12b is connected with gate signal line 17a of a bottom of screen. As an arrow head A also shows the scanning direction of the gate signal line 17, it is the direction of the upper part of a screen to the lower part. In addition, the source signal line 18 is common to the screen upper part and a bottom of screen.

[0286] In drawing 29, it connects so that gate driver 12a may differ from the gate signal line 17 by which the screen upper part adjoined. Gate driver 12a is connected with the odd-numbered gate signal line b. Moreover, gate driver 12b is connected with even-numbered gate signal line 17a. Gate signal line 17b of the scanning direction of a gate signal line is the direction of the screen upper part to the lower part (arrow head A). Gate signal line 17a is the direction of a bottom of screen to the upper part (arrow head B). Thus, by connecting the gate signal line 17 with a gate driver IC 12, by making the scan method of a gate signal line into a predetermined direction, a brightness inclination does not occur on Screen 21, but generating of a flicker can also be controlled again.

[0287] In addition, the source signal line 18 is common to the screen upper part and a bottom of screen. However, it cannot be overemphasized that you may divide by the upper and lower sides of a screen. The above matter is applied to other examples.

[0288] Gate driver 12a is connected with gate signal line 17b of the screen upper part in drawing 30. Moreover, gate driver 12b is connected with gate signal line 17a of a bottom of screen. The scanning direction of gate signal line 17b is the direction of the upper part of a screen to the lower part, as an arrow head A shows. The scanning direction of gate signal line 17a is the direction of the lower part of a screen to the upper part, as an arrow head B shows. In addition, the source signal line 18 is common to the screen upper part and a bottom of screen. Thus, by connecting the gate signal line 17 with a gate driver IC 12, by making the scan method of a gate signal line into a predetermined direction, a brightness inclination does not occur on Screen 21, but generating of a flicker can also be controlled again.

[0289] Moreover, in drawing 30, the source driver IC 14 and the gate driver IC 12 are formed into 1 chip (1 chip driver IC14a). If 1 chip is formed, mounting of IC chip to a display panel 82 can be managed with one piece. Therefore, mounting cost can also be reduced. Moreover, the various electrical potential differences used within 1 chip driver IC can also be generated in coincidence. It cannot be overemphasized that 1 chip driver IC14a may be produced with semi-conductor wafers, such as silicon, it may not limit to this although mounted in a display panel 82, and you may form in a display panel 82 directly with a low-temperature polish recon technique and an elevated-temperature polish recon technique. Moreover, it cannot be overemphasized that the driver IC which drives the upper part of a screen may be arranged to the surface of a display screen, and the driver IC which drives the lower part of a screen may be arranged the lower side of a display screen (that is, Mounting IC serves as two chips). The above matter is applied also to the example of other this inventions.

[0290] Although it expressed in drawing 28 and drawing 30 so that a screen might be divided in the center section, it does not limit to this. For example, in the case of drawing 28, display screen 21a may be made small, and it may enlarge display screen 21b. Let display screen 21a be a partialness viewing area (refer to the drawing 110). A partialness viewing area mainly performs a time stamp and the date display. Moreover, a partialness viewing area is used in low-power mode. In drawing 28 and drawing 30, viewing-area 21a is displayed by gate signal line 17b, and viewing-area 21b is displayed by gate signal line 17a.

[0291] Moreover, it is good in drawing 110 also as a configuration which considers viewing-area 21a as a configuration free three sides, and arranges the conventional source driver 14 and a conventional gate driver 12 for viewing-area 21b the separate side so that it may illustrate in drawing 111. That is, gate signal line 17a and source signal-line 18a are outputted from 1 chip driver IC14a.

[0292] Moreover, a viewing area 21 may be divided into two fields, 21a and 21b, so that it may illustrate to drawing 114, and the source driver IC 14 corresponding to each field and a gate driver 12 may be arranged. Since the write-in time amount of the video signal outputted from each source driver 14 in drawing 114 doubles as compared with other examples, a signal can fully be written in a pixel. Moreover, the viewing area 21 is set to one and may arrange the source driver IC 14 of a screen whose number is one each up and down so that it may illustrate to drawing 113. This is applicable similarly to a gate driver IC 12.

[0293] In addition, although it was the configuration of the above example having formed the gate signal line 17 in parallel, and wiring to a pixel field, it cannot be overemphasized that the source signal line 18 may be constituted so that it may wire in parallel with one side so that it may not limit to this and may illustrate to drawing 112.

[0294] In drawing 110, drawing 111, drawing 114, etc., it is also a means effective in low-power-izing to change a frame rate (drive frequency or count of screen rewriting of per unit time amount (for 1 second)) by viewing areas 21a and 21b. Moreover, it is also effective in low-power-izing to change the number of foreground colors or a foreground color by viewing areas 21a and 21b.

[0295] The cathode of EL element 15 is connected to Vs1 potential with the configuration

illustrated by drawing 1. However, there is a problem that the driver voltages of the organic electroluminescence which constitutes each color differ. for example, green, although the terminal voltage of an EL element is 5 (V) in blue (B) when the current per [0.01] unit square centimeter (A) is passed -- in (G) and red (R), it is 9 (V). That is, terminal voltage differs by B, G, and R. Therefore, in B, G, and R, the source-drain electrical potential differences (SD electrical potential difference) of 11c11d of transistors to hold differ. Therefore, the off leakage current between source-drain electrical potential differences (SD electrical potential difference) of a transistor will differ in each color. If off leakage current occurs and off leak properties differ in each color, it will become about the complicated display condition which a flicker generates after color balance has shifted that correlate with the luminescent color and a gamma property shifts.

[0296] Since this technical problem is coped with, it constitutes from this invention so that it may illustrate to drawing 5, and the potential of one cathode electrode may be changed with the potential of the cathode electrode of other colors among R, G, and B color at least. By drawing 5, B is set to cathode electrode 53a, and, specifically, G and R are set to cathode electrode 53b. In addition, although drawing 5 assumes the bottom ejection which takes out light from a glass side, there is also a case of upper ejection. In this case, a cathode and an anode may become the reversed configuration.

[0297] It cannot be overemphasized that it is desirable to make it in agreement as much as possible as for the terminal voltage of EL element 15 of R, G, and B. At least, white peak brightness is displayed, and in the or more 6000K9000K or less range, a color temperature needs to carry out an ingredient or structure selection so that the terminal voltage of the EL element of R, G, and B may become below 10 (V). moreover, ** of R, G, and B -- it is necessary to **** the difference of the greatest terminal voltage of an EL element, and the minimum terminal voltage within 2.5 (V) inside It is necessary to carry out to below 1.5 (V) still more preferably. In addition, in the above example, although the color was set to RGB, it is not limited to this. This is explained later.

[0298] Moreover, color nonuniformity also needs to be amended. This is generated by the variation in thickness, and the variation of a property in order to distinguish EL ingredient of each color by different color with. In order to amend this, white raster display is performed by 70% of brightness 30%, and the field internal division cloth of each color in a viewing area 21 is measured. Field internal division cloth is measured by a unit of one point to at least 30 pixels. This measurement data is saved on the table which consists of memory, and this saved data is used, and it constitutes so that input image data may be amended and it may display on the display screen 21.

[0299] In addition, although a pixel is made into the three primary colors of R, G, and B, it may not be limited to this, and three colors of cyanogen, yellow, and magenta are sufficient as it. Moreover, two colors of B and yellow are sufficient. Of course, monochrome is sufficient. Moreover, six colors of R, G, B, cyanogen, yellow, and magenta are sufficient. Five colors of R, G, B, cyanogen, and magenta are sufficient. The color reproduction range expands these as a natural color, and they can realize a good display. In addition, four colors of R, G, B, and white are sufficient. Moreover seven colors of R, G, B, cyanogen, yellow, magenta, black, and white are sufficient, the pixel of white luminescence is formed in the viewing-area 21 whole (production), and it is good also as a three-primary-colors display at color filters, such as RGB. In this case, what is necessary is to carry out the laminating of the luminescent material of each color, and just to form it in EL layer. Moreover, 1 pixel may be distinguished by different color with like B and yellow. EL display of this invention is not limited to what performs color display by the three primary colors of RGB as mentioned above.

[0300] There are mainly three methods in colorization of an organic electroluminescence

display panel, and a color conversion method is one of these. Remaining green and red required for full-color-izing are made by color conversion from blue glow that what is necessary is just to form the monolayer of a blue chisel as a luminous layer. Therefore, there is an advantage which does not need to distinguish each class of RGB by different color with that it is not necessary to prepare the organic electroluminescence ingredient of each color of RGB. A color conversion method is distinguished by different color with, and it does not have a ********** fall so that it may be a method. The EL panel of this invention etc. is applied by any of this method.

[0301] Moreover, pixel 16W of white luminescence may be formed in everything but the three primary colors so that it may illustrate to drawing 168. Pixel 16W of white luminescence are realizable by producing from that of carrying out the laminating of the structure of R, G, and B luminescence (formation or configuration). 1 set of pixels serve as the three primary colors of RGB from pixel 16W of white luminescence. It becomes easy to express white peak brightness by forming the pixel of white luminescence. therefore, there is a feeling of brightness -- image display implementation can be carried out.

[0302] As for the area of the pixel electrode of each color, it is desirable to make it differ so that the three primary colors, such as RGB, may be illustrated to drawing 169, even if it is the case where 1 set of pixels are carried out. Of course, balance of the luminous efficiency of each color may be good, and the same area is sufficient as long as balance also avoids color purity. However, if the balance of one or more colors is bad, it is desirable to adjust a pixel electrode (luminescence area). The electrode surface product of each color should just determine current density as criteria. That is, when a color temperature adjusts a white balance in the 9000K or less range more than 6000K (kelvin), it is made for the difference of the current density of each color to become less than **30%. It is made to become less than **15% still more preferably. if current density carries out 100A / square meter -- the three primary colors -- each -- 70A / square -- more than meter -- 130A / square -- it is made to become below meter further -- desirable -- the three primary colors -- each -- 85A / square -- more than meter -- 115A / square -- it is made to become below meter

[0303] Moreover, it is desirable to arrange in the adjoining pixel line, so that arrangement in three primary colors may differ so that it may illustrate to drawing 170. For example, from the left, if the eventh line is arrangement of R, G, and B, it will consider the oddth line as arrangement of B, G, and R. Thus, by arranging, the resolution of the direction of slant of an image is improved also with the small number of pixels. Furthermore, pixel arrangement may be changed above a 3-pixel line so that the 1st line may be considered as arrangement of R, G, B, R, G, and B from the left, the 2nd line may be considered as arrangement of G, B, R, G, B, and R and the 3rd line may be considered as arrangement of B, R, G, B, R, and G.

[0304] Cathode electrode 53a is formed using the metal mask technique which distinguished the organic electroluminescence of each color by different color with. A metal mask is used because organic electroluminescence cannot perform etching etc. in water weakly. Using a metal mask (not shown), cathode electrode 53a is vapor-deposited and connection is taken by contact hole 52a to coincidence. B cathode wiring 51a and electrical installation can be taken by contact hole 52a.

[0305] Cathode electrode 53b is similarly formed using the metal mask technique which distinguished the organic electroluminescence of each color by different color with. Using a metal mask (not shown), cathode electrode 53b is vapor-deposited and connection is taken by contact hole 52b to coincidence. RG cathode wiring 51b and electrical installation can be taken by contact hole 52b. In addition, the aluminum thickness of a cathode electrode is good to form so that it may be set to 70nm or more 200nm or less.

[0306] Since a different electrical potential difference can be impressed to the cathode electrodes 51a and 51b by the above configuration, even if the Vdd electrical potential

difference of drawing 1 is common to each color, the electrical potential difference impressed to EL of at least 1 color among RGB can be changed. In addition, at drawing 5, although referred to as the same cathode electrode 53b, it may not limit to this, and you may constitute from RG so that it may become a cathode electrode which is different by R and G.

[0307] By constituting as mentioned above, the OFF leakage current between the source-drain electrical potential differences (SD electrical potential difference) of a transistor can prevent generating and a kink phenomenon in each color. Therefore, a flicker does not have generating, it does not correlate with the luminescent color, a gamma property does not necessarily shift, and good image display can be realized.

[0308] Moreover, it cannot be overemphasized that it may not limit to this although [this cathode electrical potential difference] Vsl of drawing 1 is made into a cathode electrical potential difference and it is made to differ in each color, and the anode electrical potential difference Vdd may be constituted so that it may differ in each color. For example, it is the configuration which makes Vdd of the pixel of R an electrical potential difference 8 (V), sets G to 6 (V) and sets B to 10 (V). As for these anode electrical potential differences and a cathode electrical potential difference, it is desirable to constitute so that it can adjust in **1 (V).

[0309] Even if panel size is about 2 inches, about 100mA current is outputted from the anode connected with Vdd. Therefore, the reduction in resistance of the anode wiring 20 (current supply source line) is indispensable. Since this technical problem is coped with, by this invention, anode 63 wiring is supplied from viewing-area a top and the bottom so that it may illustrate by drawing 6 (both-ends electric supply). Generating of the brightness inclination by the upper and lower sides of a screen is lost by carrying out both-ends electric supply as mentioned above.

[0310] In order to raise luminescence brightness, it is good to carry out surface roughening of the pixel 48. This configuration is shown in drawing 7. First, the La Stampa technique is used for the part which forms the pixel electrode 48, and detailed irregularity is formed in it. When a pixel is a reflective mold, the metal thin film of about 200nm aluminum is formed by the sputtering method, and the pixel electrode 48 is formed. Surface roughening of the heights is prepared and carried out to the part where the pixel electrode 48 touches organic electroluminescence. In addition, in the case of a simple matrix type display panel, the image electrode 48 makes it the shape of a stripe-like electrode. Moreover, heights may not be limited only to convex and a concave is sufficient as them. Moreover, concave and a convex may be formed in coincidence.

[0311] Magnitude of a projection was made into the diameter of about 4 micrometers, set the average of the distance between contiguity to 10 micrometers, 20 micrometers, and 40 micrometers, and performed the 120 measurement of luminance /for the unit area consistency of a projection as 800 pieces/a square millimeter from 2,600 mm from 1200 pieces/the square millimeter from 1000, and 100, respectively. Then, it turned out that luminescence brightness becomes strong, so that the unit area consistency of a projection became large. Therefore, it turned out that the surface state of a pixel electrode is changed and luminescence brightness can be adjusted by changing the unit area consistency of the projection on the pixel electrode 48. According to examination, the good result was able to be obtained for the unit area consistency of a projection by below 800 piece / below square millimeter 100 piece /, and square millimeter.

[0312] Organic electroluminescence is a self-light emitting device. If the light by this luminescence carries out incidence to TFT as a switching element, a phot conductor phenomena (contest the phot) will occur. In contest a phot, the phenomenon whose leak (off leak) in the time of OFF of switching elements, such as TFT, increases by optical pumping is said.

[0313] In order to cope with this technical problem, as shown in drawing 9, by this invention, the lower layer of a gate driver 12 (depending on the case, it is the source driver 14) and the lower layer light-shielding film 91 of the pixel transistor 11 are formed. A light-shielding film 91 is formed with metal thin films, such as chromium, and sets the thickness to 50nm or more 150nm or less. If thick [when thickness is thin, the protection-from-light effectiveness is scarce, and], irregularity will occur and patterning of upper TFT 11A1 will become difficult.

[0314] Smoothing film 71a which consists of or more 20 an inorganic material 100nm or less is formed on a light-shielding film 91. One electrode of storage capacitance 19 may be formed using the layer of this light-shielding film 91. In this case, as for smooth film 71a, it is desirable to enlarge capacity value of structure storage capacitance thinly as much as possible. Moreover, a light-shielding film 91 may be formed with aluminum, an oxidation silicone film may be formed in the front face of a light-shielding film 91 using an anodic oxidation technique, and this oxidation silicone film may be used as a dielectric film of storage capacitance 19. On smoothing film 71b, the pixel electrode of high aperture (HA) structure is formed.

[0315] The driver circuit 12 etc. should control not only a rear face but penetration of the light from a front face. It is because it malfunctions under the effect of contest a phot. Therefore, in this invention, when a cathode electrode is a metal membrane, a cathode electrode is formed also in front faces, such as a driver 12, and this electrode is used as a light-shielding film.

[0316] However, if a cathode electrode is formed on a driver 12, malfunction of the driver by the electric field from this cathode electrode or electric contact of a cathode electrode and a driver circuit may occur. In order to cope with this technical problem, in this invention, at least one layer of organic electroluminescence film of two or more layers is preferably formed on a driver circuit 12 etc. at the organic electroluminescence film formation on a pixel electrode, and coincidence.

[0317] Fundamentally, since the organic electroluminescence film is an insulating material, between a cathode and a driver is isolated by forming the organic electroluminescence film on a driver. Therefore, the above-mentioned technical problem is cancelable.

[0318] If between the terminals of one or more TFT(s)11 of a pixel, or TFT11 and a signal line short-circuit, EL element 15 may always serve as the luminescent spot to turn on. Since this luminescent spot is visually conspicuous, it is necessary to sunspot-ize it (astigmatism LGT). To the luminescent spot, the applicable pixel 16 is detected, laser light is irradiated at a capacitor 19, and between the terminals of a capacitor is short-circuited. Therefore, since it becomes impossible to hold a charge to a capacitor 19, TFT11a cannot pass a current and can carry out it.

[0319] In addition, the location which irradiates laser light is corresponded to. It is desirable to remove the cathode film. It is for preventing that the terminal electrode and cathode film of a capacitor 19 short-circuit by laser radiation.

[0320] Moreover, the structure illustrated to drawing 175 is also illustrated. Drawing 175 is the example of the Shimo ejection structure which takes out light from a glass substrate 49 side. Also in drawing 175, the lower layer of a gate driver 12 (depending on the case, it is the source driver 14) and the lower layer light-shielding film of the pixel transistor 11 are formed. A light-shielding film is formed with metal thin films, such as chromium, and the thickness is set to 50nm or more 150nm or less. If thick [when thickness is thin, the protection-from-light effectiveness is scarce, and], irregularity will occur and patterning of upper TFT 11A1 will become difficult.

[0321] On a light-shielding film, TFT11 and a driver circuit 12 (14) are formed. The driver circuit 12 (14) etc. should control not only a rear face but penetration of the light from a front

face. It is because it malfunctions under the effect of contest a phot. Therefore, in this invention, the cathode electrode 46 is used as a light-shielding film.

[0322] However, if a cathode electrode is formed on a driver 12 (14), malfunction of the driver by the electric field from this cathode electrode or electric contact of a cathode electrode and a driver circuit may occur. In order to cope with this technical problem, in this invention, at least one layer of organic electroluminescence film of two or more layers is preferably formed on a driver circuit 12 etc. at the organic electroluminescence film formation on a pixel electrode, and coincidence.

[0323] When it is the structure (it is upper ejection to take out light from Shimo drawing and EL film vacuum evaporationo side for taking out light from a glass substrate 49 side) of the Mitsukami ejection which considers a pixel electrode as a reflective type and uses a common electrode as transparent electrodes (ITO, IZO, etc.) on the other hand when a cathode (or anode) electrode is a transparent electrode, the sheet resistance of a transparent electrode poses a problem. Although a transparent electrode is high resistance, it is necessary to pass a current with high current density to the cathode of organic electroluminescence. If it carries out and backlash forms a cathode electrode by the monolayer of the ITO film, it will be in a heating condition by generation of heat, or the brightness inclination of the degree of pole occurs in the display screen.

[0324] Since this technical problem is coped with, the low resistance-ized wiring 92 which consists of a metal thin film is formed in the front face of a cathode electrode. The low resistance-ized wiring 92 is the same configuration (it is 50nm - 200nm thickness with chromium or an aluminum ingredient) as the black matrix (BM) of a liquid crystal display panel, and is the same locations (on pixel inter-electrode and a driver 12 etc.). However, in organic electroluminescence, since it is not necessary to form BM, functions completely differ. In addition, the low resistance-ized wiring 92 may not be limited to the front face of a transparent electrode 72, and may be formed in a rear face (field which touches the organic electroluminescence film). Moreover, an alloy or the laminating structures, such as Mg-Ag, Mg-Li, and aluminum-Li, etc. may use aluminum, magnesium, an indium, copper, or each alloy as a metal membrane formed in the shape of BM. In addition, in order to prevent corrosion etc. on BM, the laminating of ITO and the IZO film is carried out further, and organic thin films, such as inorganic thin films, such as SiNx and SiO2, or polyimide, are formed.

[0325] Moreover, as for the case in the case (upper ejection) of taking out light from the vacuum evaporationo side of EL film, it is desirable to form the Mg-aluminum film on the organic electroluminescence film 47, and to form ITO and the IZO film on it. Moreover, it is desirable to form the Mg-aluminum film on the organic electroluminescence film 47, and to form a black matrix (a black matrix like a liquid crystal display panel) on it. As for this black matrix, it is desirable to form by chromium, aluminum, Ag, Au, Cu, etc., and to form on this the protective coat which consists of organic compound insulators, such as inorganic insulator layers, such as SiO2 and SiNx, polyester, and an acrylic. Furthermore, an antireflection film (AIR coat) is formed on this protective coat.

[0326] An AIR coat has the configuration of three layers, or a two-layer configuration. In the case of 3 lamination, optical thickness carries out nd1=lambda / 4 laminatings of nd1=lambda/2 and the magnesium fluoride (MgF2) for nd=lambda/4, and a zirconium (ZrO2), and an aluminum oxide (aluminum 2O3) is formed. Usually, a thin film is formed as a value of 520nm or near of those as lambda.

[0327] optical in silicon monoxide (SiO) in a two-layer configuration -- nd1=lambda / 4 laminatings of nd1=lambda/4 or yttrium oxide (Y2O3), and the magnesium fluoride (MgF2) are carried out, and thickness nd1=lambda/4, and magnesium fluoride (MgF2) are formed.

[0328] In the case of one layer, nd1=lambda / 2 laminatings of the magnesium fluoride

(MgF2) are carried out, and it is formed.

[0329] In addition, even if it is the case of bottom ejection, it is effective to make high the permeability of the metal membrane of the cathode electrode 46. Even if it is the configuration of seeing a display image from a substrate 49 side, it is because it is high, so a reflect lump decreases the permeability of a metal membrane 46. If a reflect lump decreases, the circular polarization of light plate 74 will become unnecessary. Therefore, optical ejection effectiveness may improve rather than upper ejection. As for the permeability of a metal membrane 46, it is desirable to make it to 90% or less 60% or more. It is desirable to make it to especially 90% or less 70% or more. The sheet resistance of a cathode electrode becomes it low that it is 60% or less. However, a reflect lump becomes large. Conversely, at 90% or more, the sheet resistance of a cathode electrode becomes high. Therefore, the brightness inclination of a display image becomes large.

[0330] For making the permeability of a metal membrane 46 high, aluminum film is formed thinly. Thickness is formed in 20nm or more 100nm or less. It is desirable to form ITO and the IZO film on it. Moreover, it is desirable to form a black matrix on the aluminum film 46. As for this black matrix, it is desirable to form by chromium, aluminum, Ag, Au, Cu, etc., and to form on this the protective coat 1761 which consists of organic compound insulators, such as inorganic insulator layers, such as SiO2 and SiNx, polyester, and an acrylic. Furthermore, it is desirable to form an antireflection film (AIR coat) on this protective coat 1761.

[0331] The luminescence area of the EL film 47 becomes large by making the pixel electrode 48 into the shape of radii so that it may illustrate to drawing 176. Therefore, current density becomes small and high life-ization of EL element 47 can be realized. Moreover, since the terminal voltage of EL element 15 also falls, power efficiency also improves.

[0332] In drawing 176, the smoothing film 71 is formed in the shape of radii, and the contact hole which takes the drain terminal of TFT11 and contact on the smoothing film of the shape of these radii is formed. The transparent electrode 48 and drain terminal which consist of ITO in this contact hole are connected electrically.

[0333] 50nm or more carbon film 150nm or less is thinly vapor-deposited on the pixel electrode 48, and the EL film 47 is formed on this. In the case of monochrome, on the whole surface, in the case of RGB, a metal mask is used, and the EL film 47 distinguishes it by different color with (refer to drawing 177 (f)).

[0334] The aluminum film 46 used as a cathode electrode is formed after formation of the EL film 47 (drawing 177 (g)). Furthermore, a protective coat 1761 is formed on the aluminum film 46 (drawing 177 (h)).

[0335] In addition, the EL film 47 or the pixel electrode 48 may not be limited in the shape of radii, and the shape of the shape of a triangular pyramid and a cone and the letter of a sign curve are sufficient as it, and the structure which combined these is sufficient as it. Moreover, you may be the configuration that the shape of the shape of a triangular pyramid and a cone and the letter of a sign curve should have been formed, these had combined enough, or random irregularity was formed, on radii detailed to 1 pixel. moreover -- drawing 176 -- convex -- being circular -- although -- a concave -- being circular . The above matter is the same also with the structure which the shape of the shape of a triangular pyramid and a cone and the letter of a sign curve are sufficient as, and combined these.

[0336] Drawing 177 is an explanatory view of the manufacture approach of EL display panel explained in drawing 176. TFT11, the gate driver circuit 12, etc. are formed on the array substrate 49 so that it may illustrate in drawing 177 (a).

[0337] Next, the smoothing film 71 which consists of organic materials, such as acrylic resin, is applied on a substrate 49 so that it may illustrate to drawing 177 (b). In addition, the smoothing film 71 may be inorganic materials, such as SOG. As for thickness, it is desirable

to make it 1.5 micrometers or more 3 micrometers or less. Next, a mask 1771 is formed on said smoothing film 71. A mask 1771 is formed with a metallic material and it is made for a formation location to correspond to a pixel 16. Next, it etches. Any of dry etching, such as wet etching and O2 plasma, are sufficient as etching. The smoothing film 71 is etched from between masks 1771. Therefore, the smoothing film 71 becomes circular so that it may illustrate to drawing 1771 (c).

[0338] Furthermore, a mask (not shown) is formed in the smoothing film 71, and a contact hole 1772 is formed so that it may illustrate to drawing 177 (d). Or a contact hole 1772 is also formed in coincidence at the etching process of drawing 177 (b).

[0339] Next, the pixel electrode 48 is formed with transparent electrodes, such as ITO and IZO, so that it may illustrate to drawing 177 (e). The pixel electrode 48 and TFT11 take connection in the pixel contact section 1751. The transparent electrode 48 and drain terminal which consist of ITO in this contact hole are connected electrically.

[0340] 50nm or more carbon film 150nm or less is thinly vapor-deposited on the pixel electrode 48, and the EL film 47 is formed on this. In the case of monochrome, on the whole surface, in the case of RGB, a metal mask is used, and the EL film 47 distinguishes it by different color with (refer to drawing 177 (f)). The aluminum film 46 used as a cathode electrode is formed after formation of the EL film 47 (drawing 177 (g)). Furthermore, a protective coat 1761 is formed on the aluminum film 46 (drawing 177 (h)).

[0341] For making the permeability of a metal membrane 46 high, the aluminum film 46 is formed thinly. Thickness is formed in 20nm or more 100nm or less. It is desirable to form ITO and the IZO film on it. Moreover, it is desirable to form a black matrix on the aluminum film 46. As for this black matrix, it is desirable to form by chromium, aluminum, Ag, Au, Cu, etc., and to form on this the protective coat 1761 which consists of organic compound insulators, such as inorganic insulator layers, such as SiO2 and SiNx, polyester, and an acrylic. Furthermore, it is desirable to form an antireflection film (AIR coat) on this protective coat 1761. In addition, the minimum thickness of a protective coat 1761 is set to 1 micrometers or more.

[0342] A protective coat 1761 may be the protective layer which used the film. For example, using for the film of an electrolytic capacitor what vapor-deposited DLC (diamond- -like carbon) as a protective layer is illustrated. This film has very bad moisture permeability (moisture proof). This film is carried out protective layer 1761, and is used.

[0343] The thickness of a protective layer 1761 is n-d (n calculates those refractive indexes by making them synthesis (n-d of each thin film being calculated), when the laminating of the refractive index of a thin film and two or more thin films is carried out.). d synthesizes and calculates those refractive indexes, when the laminating of the thickness of a thin film and two or more thin films is carried out. It is good to make it become below the luminescence dominant wavelength lambda of EL element 15.

[0344] Drawing 178 is a panel-ized block diagram (sectional view). although other drawings are the same, in order that [in addition,] each drawing may make a plot easy easily [understanding] in this specification -- an abbreviation -- or/and, enlarging or contracting is carried out. Also in the sectional view of the display panel of drawing 178, the smoothing film 71 etc. is illustrated thickly enough. However, board thickness is also illustrating the substrate 49 very thinly. Moreover, TFT etc. is omitting and illustrating.

[0345] In drawing 178, a spacer 1781 is arranged between the closure plate 41 and a substrate 49, and it is constituted so that a protective coat 1761, the reflective film 46 or the EL film 47, and the closure plate 41 may not touch directly. The periphery of a viewing area is arranged or filled up with the drying agent. A spacer uses cylinder-like a thing or a spherical thing. As for height, it is desirable to make it 10 micrometers or more 100 micrometers or less. Moreover, it can also consider as a spacer by processing a protective coat 1761. That is, the

function of a spacer is given from that of processing or forming a part or all of a protective coat 1761 a letter of projection, or column top, or in the shape of a stripe. In addition, the configuration which uses a spacer 1781 as a drying agent is also desirable.

[0346] TFT11b and TFT11a of the pixel shown in drawing 21 are the relation of a current mirror. The properties (a threshold Vt, S value, mobility mu, etc.) of 11b and 11a of the relation of this current mirror must be in agreement. Moreover, in the pixel of drawing 1, it cannot be overemphasized that it is desirable that each property of TFT is in agreement.

[0347] As for the semi-conductor film which constitutes TFT11 of a pixel 16, in a low-temperature polish recon technique, forming by laser annealing is common. The variation in the conditions of this laser annealing turns into variation in TFT11 property. However, by the method which performs current programs, such as drawing 1, drawing 21, drawing 22, drawing 43, and drawing 71, if the property of TFT11 in 1-pixel 16 is in agreement, it can drive so that a predetermined current may flow to EL element 15. This point is an advantage which is not in an electrical-potential-difference program.

[0348] To this technical problem, by this invention, as shown in drawing 23, the laser radiation spot 23 at the time of annealing is irradiated in parallel with the source signal line 18. Moreover, the laser radiation spot 23 is moved so that it may be in agreement with a 1-pixel train. Of course, 1 pixel may irradiate laser in the unit [RGB / not the thing to limit to a 1 pixel train but / of drawing 23] 16 (in this case, it will be called a 3-pixel train).

[0349] Especially the pixel is produced so that it may become a square configuration by 3 pixels of RGB. Therefore, each pixel of R, G, and B serves as a longwise pixel configuration. Therefore, arrangement of TFT11 formed in a pixel 16 is arranged in a lengthwise direction so that it may illustrate to drawing 23 (TFT(s) 11a and 11b). Therefore, the property variation of TFT11 can be prevented from generating within 1 pixel by making the laser radiation spot 23 longwise and annealing it.

[0350] Generally the die length of the laser radiation spot 23 is a fixed value like 10 inches. Since this laser radiation spot 23 is moved, it is necessary to arrange a panel so that it may fall within the range which can move one laser radiation spot 23 (that is, are and it carries out so that the laser radiation spot 23 may not lap in the center section of the viewing area 21 of a panel).

[0351] With the configuration of drawing 24, it is formed so that three panels may be perpendicularly arranged within the limits of the die length of the laser radiation spot 23. The annealer which irradiates the laser radiation spot 23 recognizes positioning marker 242a of a glass substrate 241, and 24ab, and moves the laser radiation spot 23. Pattern recognition equipment performs recognition of the positioning marker 242. An annealer (not shown) recognizes the positioning marker 242 and deduces the location of a pixel train. And exactly, the laser radiation spot 23 is irradiated and annealing is performed one by one so that it may lap with a pixel aisle location.

[0352] As for especially the laser annealing approach (method which irradiates a laser Rhine-like spot in parallel with the source signal line 18) explained by drawing 23 and drawing 24, it is desirable to adopt at the time of the current program method of an organic EL panel. Because, it is because the property of TFT11 is in agreement in a source signal line in parallel (the property of the pixel TFT which adjoined the lengthwise direction approximates). Therefore, there is little change of the voltage level of a source signal line at the time of a current drive, and it is hard to generate current write-in lack at it (for example, if it is white raster display, since the current passed to TFT11a of each pixel which adjoined is almost the same, there is little change of the current amplitude outputted from the source driver IC 14).

[0353] Moreover, homogeneity can realize image display (it is because it is hard to generate the display nonuniformity which originates mainly in dispersion in a TFT property) by the method which carries out the coincidence writing of two or more pixel lines explained by

drawing 87, drawing 88, etc. Since drawing 87 etc. is chosen as two or more pixel line coincidence, if its TFT of the pixel which adjoined is uniform, the TFT property nonuniformity of a lengthwise direction is absorbable in a driver circuit 14.

[0354] As shown in drawing 1, gate signal line 17a will be in switch-on (since the transistor 11 of drawing 1 is a p channel transistor here, it is flowed with a low level) at a line selection period, and gate signal line 17b is taken as switch-on at the time of a non-selection period.

[0355] If the parasitic capacitance of the source signal line 18 increases as it is shown in drawing 55 (a), when the condition of a source signal line is in a gradation 0 display condition, the current value over gradation 1 is impressed and a line selection period is operated in 75 microseconds, the current value outputted to EL element 15 will decrease.

[0356] Drawing 55 (b) is the case where the current value over gradation 1 is passed 10 times compared with (a), and the reduction rate of the current value outputted to EL element 15 to the increment in the parasitic capacitance of the source signal line 18 becomes small.

[0357] Since about 10% of dispersion cannot be observed as a difference of brightness for human being's eyes to a predetermined current value, the source capacity permitted supposing it accepts about 10% of fall is 25pF or less in (a) 2pF or less and 8 (b).

[0358] Since the time amount t which current value change of the source signal line 18 takes is t=C·V/I when the current which flows the electrical potential difference of C and a source signal line to V and a source signal line in the magnitude of stray capacity is set to I, that a current value can be enlarged 10 times can do short time amount which current value change takes to about 1/10. Or even if source capacity increases 10 times, it is shown that it can change to a predetermined current value. Therefore, in order to write in a predetermined current value within a short horizontal scanning period, it is effective to make a current value increase.

[0359] Since the output current will also become 10 times and the brightness of EL will become 10 times, if an input current is increased 10 times, in order to obtain predetermined brightness, predetermined brightness was displayed by setting a transistor 17d [of drawing 1] "on" period to 1/10 over the past, and setting a luminescence period to 1/10.

[0360] That is, in order to fully perform the charge and discharge of the parasitic capacitance of the source signal line 18 and to perform a program for a predetermined current value to TFT11a of a pixel 16, it is necessary to output a comparatively big current from the source driver 14. However, if a big current in this way is passed to the source signal line 18, this current value will be programmed by the pixel, and a big current flows to EL element 15 to a predetermined current. For example, if it programs with a 10 times as many current as this, naturally, a 10 times as many current as this will flow to EL element 15, and EL element 15 will emit light by one 10 times the brightness of this. What is necessary is just to make into 1/10 time amount which flows to EL element 15, in order to make it predetermined luminescence brightness. Thus, by driving, the charge and discharge of the parasitic capacitance of the source signal line 18 can fully be carried out, and predetermined luminescence brightness can be obtained.

[0361] In addition, this is an example, although one 10 times the current value of this is written in TFT11a (the terminal voltage of a capacitor 19 is set up correctly) of a pixel and ON time amount of EL element 15 is made into 1/10. Depending on the case, one 10 times the current value of this is written in TFT11a of a pixel, and it is good as for 1/5 in the ON time amount of EL element 15. Conversely, one 10 times the current value of this may be written in TFT11a of a pixel, and the ON time amount of EL element 15 may be doubled. This invention has the description in making the write-in current to a pixel into values other than a predetermined value, making into an intermittent condition the current which flows to EL element 15, and driving. On these specifications, in order to give explanation easy, one N times the current value of this is written in TFT11 of a pixel, and it explains increasing the

ON time amount of EL element 15 1/N time. However, not the thing to limit to this but a current value 1 time the N of this is written in TFT11 of a pixel, and it cannot be overemphasized that twice (it differs in N1 and N2) as many 1-/N as this is sufficient in the ON time amount of EL element 15. In addition, spacing which carries out an intermission is not limited at equal intervals. For example, random is sufficient (a display period or a non-display period should just serve as a predetermined value (fixed comparatively) as a whole). Moreover, you may differ by RGB. That is, what is necessary is just to adjust so that white (White) balance may become the optimal, and R, G, a B display period, or a non-display period may serve as a predetermined value (fixed comparatively) (setup).

[0362] Moreover, in order to give explanation easy, 1-/N is explained setting these 1F to 1-/N on the basis of 1F (1 field or one frame). However, a 1-pixel line is chosen, and there is time amount (usually 1 horizontal-scanning period (1H)) by which a current value is programmed, and an error is also produced depending on a scan condition. Therefore, the above explanation is only the problem of the shape of facilities for giving explanation easy to the last, and is not limited to this.

[0363] Organic (inorganic) EL indicating equipment has a technical problem also in the point that the method of presentation differs from the display which displays an image as a set of a line display with an electron gun like CRT fundamentally. That is, in EL display, the current (electrical potential difference) written in the pixel is held between the periods of 1F (1 field or one frame). Therefore, if a movie display is performed, the technical problem that profile dotage of a display image occurs will occur.

[0364] In this invention, during the period of 1 F/N **** a current to EL element 15, and other periods (1F (N-1) / N) do not pass a current. The case where carried out this drive method and one point of a screen is observed is considered. In this display condition, image data display and a black display (astigmatism LGT) are repeatedly displayed on every 1F. That is, an image data display condition will be in a discontinuous display (intermittent display) condition in time. If animation data display is seen in the state of this intermittent display, profile dotage of an image is lost and a good display condition can be realized. That is, animation display near CRT is realizable. Moreover, although an intermittent display is realized, the Maine clock of a circuit is not different from the former. Therefore, the power consumption of a circuit does not increase.

[0365] The image data (electrical potential difference) to which light modulation is carried out in the case of a liquid crystal display panel is held at a liquid crystal layer. Therefore, if it is going to carry out a black insertion display, it is necessary to rewrite the data currently impressed to a liquid crystal layer. Therefore, it is necessary to make high the clock of the source driver IC 14 of operation, and to impress a black indicative data to the source signal line 18 for image data by turns. Therefore, if black insertion (intermittent display of a black display etc.) is made into implementation ******, it is necessary to raise the Maine clock of a circuit. Moreover, the image memory for carrying out time-axis elongation is also needed.

[0366] With the pixel configuration of EL display panel of this invention shown in drawing 78 etc., image data is held at the capacitor 19 from drawing 1, drawing 43, drawing 44, drawing 53, drawing 54, and drawing 67. The current corresponding to the terminal voltage of this capacitor 19 is passed to EL element 15. Therefore, image data is not held like a liquid crystal display panel at a light modulation layer.

[0367] This invention controls the current passed to EL element 15 only by making TFT11d of switching, or TFT11e turn on and off. That is, even if it turns off the current Iw which flows to EL element 15, as for image data, the capacitor 19 is held as it is. Therefore, if 11d of switching elements etc. is made to turn on to the following timing and a current is passed to EL element 15, the flowing current is the same as that of the current value which was flowing before. If black insertion (intermittent display of a black display etc.) is made into

implementation ******, it is not necessary to raise the Maine clock of a circuit with this invention in the case. Moreover, the image memory for not carrying out time-axis elongation is also unnecessary. Moreover, time amount after an organic EL device 15 impresses a current until it emits light is a high-speed response short. Therefore, it is suitable for a movie display and the problem of the movie display which is the problem of the display panels (a liquid crystal display panel, EL panel, etc.) of the conventional data-hold mold can be solved from that of carrying out an intermittent display further.

[0368] For example, as shown in drawing 33, for gate signal line 17b, an "on" period is 1F (since program time is usually 1H and the pixel line count of EL display is at least 100 or more lines when current program time is set to 0) conventionally. If it supposes that an error is 1% or less also as 1F and is referred to as N= 10, if source capacity is about 20pF, according to drawing 55, it can change from the gradation 0 which starts change most as for time amount also to gradation 1 in about 75 microseconds. If this is EL display of 2 mold extent, it shows that frame frequency can drive by 60Hz.

[0369] Furthermore, what is necessary is just to make the source current into 10 or more times, when source capacity becomes large with a large-sized display. What is necessary is just to make the "on" period of gate signal line 17b (TFT11d) into 1 F/N, when a source current value is generally increased N times. Thereby, it is applicable to the display for television and monitors etc.

[0370] Hereafter, it explains in more detail, referring to a drawing. First, the parasitic capacitance 404 of drawing 1 is generated with the joint capacity between source signal lines, the buffer output capacitance of drive IC 14, the cross capacity of the gate signal line 17 and the source signal line 18, etc. This capacity 404 is usually set to 10pF or more. In an electrical-potential-difference drive, since an electrical potential difference is impressed to the source signal line 18 by low impedance, parasitic capacitance does not become large from a driver IV14 with a problem by drive somewhat.

[0371] However, it is necessary to program the capacitor 19 of a pixel with the minute current of 5 or less nAs by the image display of black level especially at a current drive. Therefore, if parasitic capacitance 404 occurs in the magnitude beyond a predetermined value, the charge and discharge of the parasitic capacitance cannot be carried out into the time amount (since less than [1H], however a 2-pixel line may be written in coincidence, not usually limited to less than [1H].) programmed in a 1-pixel line. If charge and discharge become impossible in 1H period, it will become insufficient writing in to a pixel and resolution will not come out at all.

[0372] In the pixel configuration of drawing 1, as shown in drawing 13 (a), the program current I1 flows to the source signal line 18 at the time of a current program. 19 capacitorV1 is set up so that this current I1 may flow TFT11a and the current which passes I1 may be held (program). At this time, TFT11d is in an opening condition (OFF state).

[0373] Next, TFT11 operates like drawing 13 (b) in the period which passes a current to EL element 15. That is, OFF state voltage (Vgh) is impressed to gate signal line 17a, and TFT(s) 11a and 11c turn off. On the other hand, ON state voltage (Vgl) is impressed to gate signal line 17b, and TFT11d turns on.

[0374] Now, supposing a current I1 is N times the current (predetermined value) originally passed, the current which flows to EL element 15 of drawing 13 (b) will also be set to I1. Therefore, EL element 15 emits light with a value 10 times the brightness of predetermined.

[0375] Then, only the period of 1-/N of the time amount (about 1 F) which originally turns on TFT11d is made to turn on, and if other period (N-1) / N periods are made to turn off, the average luminance of the 1F whole will turn into predetermined brightness. This display condition is approximated with CRT scanning the screen with the electron gun. The range where a different point shows the image is the point which 1-/N (a full screen is set to 1) of

the whole screen has turned on (the range turned on in CRT is a 1-pixel line (it is 1 pixel strictly).).

[0376] In this invention, as the image display field of this 1-/N shows drawing 31 (a1), it moves downward from on Screen 21. In this invention, only in during the period of 1 F/N, a current flows to EL element 15, and other periods (1F- (N-1) / N) do not flow a current. Therefore, an image serves as an intermittent display. However, since it will be in the condition that the image was held according to the after-image at human being's eyes, it seems that the full screen is displayed on homogeneity.

[0377] In this display condition, image data display and a black display (astigmatism LGT) are repeatedly displayed on every 1F. That is, an image data display condition will be in a discontinuous display (intermittent display) condition in time. By the liquid crystal display panel (EL display panels other than this invention), since data were held at the period of 1F, and the pixel, when it was animation display, even if image data changed, the change could not be followed, but it had become animation dotage (profile dotage of an image). However, in this invention, since the image is indicated by intermittent, profile dotage of an image is lost and a good display condition can be realized. That is, animation display near CRT is realizable.

[0378] Moreover, there is also no contrast fall like [at the time of indicating the liquid crystal display panel by intermittent at EL display, since the black display was completely an astigmatism LGT]. Moreover, an intermittent display is realizable only by carrying out on-off operation of the TFT11d, as shown in drawing 13. This is because memory (the number of gradation is infinity since it is an analog value) of the image data is carried out to the capacitor 19. That is, image data is held during the period of 1F at each pixel 16. Control of TFT11d has realized whether the current equivalent to this image data currently held is passed to EL element 15.

[0379] It is important to maintain the terminal voltage of a capacitor 19. It is because flicker (flicker etc.) will occur when screen intensity changes and a frame rate falls if the terminal voltage of a capacitor 19 changes in 1 field (frame) period (charge and discharge). It is necessary to make it the current which TFT11a passes to EL element 15 in an one-frame (1 field) period not fall to at least 65% or less. In these 65%, it is that the current passed to EL element 15 when the beginning of the current passed to EL element 15 considers as 100%, just before it writes in a pixel 16, and writing in said pixel 16 with the following frame (field) considers as 65% or more.

[0380] Therefore, it is changeless to the number of TFT11 which constitutes 1 pixel from a case where it does not consider as the case where an intermittent display is realized. That is, the pixel configuration remained as it was, was removed with the effect of the parasitic capacitance 404 of the source signal line 18, and has realized the good current program. Moreover, the movie display near CRT is realized.

[0381] Moreover, since it is late enough as compared with the clock of the source driver circuit 14 of operation, as for the clock of the gate driver circuit 12 of operation, the Maine clock of a circuit does not necessarily become high. Moreover, modification of the value of N is also easy.

[0382] The direction of image display (the image write-in direction) is made down from on a screen by 1 field eye (drawing 104 (a)), and is good also as above (drawing 104 (b)) from under a screen by the following 2nd field eye so that it may illustrate to drawing 104. That is, drawing 104 (a) and drawing 104 (b) are repeated by turns.

[0383] Furthermore, once considering as down from on a screen by 1 field eye (drawing 105 (a)) and considering a full screen as the black display (non-display) 312 so that it may illustrate to drawing 105 (drawing 105 (b)), by the following 2nd field eye, it is good also as above (drawing 105 (c)) from under a screen. Moreover, it is once good also considering a

full screen as black display (non-display) 312 (drawing 105 (d)). That is, the condition of drawing 105 (a) to the drawing 105 (d) is repeated by turns.

[0384] In addition, in drawing 104, drawing 105, etc., although the approach to write in a screen was made into the top from under the bottom from a screen, it does not limit to this. Continuously, it fixes the bottom or the bottom to a top from on a screen, and the write-in direction of a screen makes down the direction of the non-display field 312 of operation from on a screen by 1 field eye, and is good also as above from under a screen by the following 2nd field eye. The above matter is the same also in the example of other this inventions.

[0385] Drawing 31 (a) sets the image display field 311 to 1-/N, and is setting the non-display field (an astigmatism LGT field, black viewing area) 312 to (N-1) / N (however, this is the case of an ideal condition.). Since there are a capacitor 19 and a thrust omission by the source-gate (SG) capacity of TFT11a actually, it differs. That is, it is the case where the image display field 311 is set to one. The image display field 311 is moved to down from on a screen, as shown in an arrow head (drawing 31 (a1) -> drawing 31 (a2) -> drawing 31 (a3) -> drawing 31 (a1) ->). However, though migration of this image display field 311 is not limited to moving to down from on a screen and moves to above from under a screen, it is good. Moreover, the 1st (1 field eye) frame is moved to down from on a screen, and it cannot be overemphasized that the following frame [2nd (2 field eye)] may be scanned so that it may move to above from under a screen (actuation). Moreover, you may scan from the right of a screen from the left or the left of a screen to the right (actuation).

[0386] Drawing 33 is a timing wave of operation. As indicated also in advance, it is supposed that it supposes that one screen is displayed in the period of 1F, and a current program will be carried out in the period of 1H. Drawing 33 (a) shows the timing wave of gate signal line 17a in drawing 1 (a) and (b). Moreover, drawing 33 (b) shows the timing wave of gate signal line 17b. when gate signal line 17b is fundamentally set to Vgl, TFT11d flows (a period is 1 F/N), a twice [N] as many current as the predetermined value I1 flows [the peak current] to EL element 15, and an EL element emits light by the brightness B (N-B) twice [N] the brightness of predetermined to it. As for the period of 1F/(N-1) / N, TFT11d will be in an OFF state.

[0387] Control of this gate signal line is easily realizable by controlling two shift registers in a gate driver 12 (22a, 22b) like drawing 2. It is because shift register 22a holds the control data of gate signal line 17a (scan) and shift register 22b should just hold the control data of gate signal line 17b (scan).

[0388] Drawing 56 shows the wave of gate signal line 17b. When drawing 56 (a) is made into the voltage waveform of gate signal line 17b of eye the 1st pixel line, the voltage waveform of gate signal line 17b of eye the 2nd pixel line adjoined eye the 1st pixel line in drawing 56 (b) is shown. Similarly, drawing 56 (c) shows the voltage waveform of the following gate signal line 17b of eye the 3rd pixel line, and drawing 56 (d) shows the voltage waveform of gate signal line 17b of eye the 4th pixel line.

[0389] As mentioned above, in each pixel line, make the same the wave of gate signal line 17b, and it is made to shift at spacing of 1H, and impresses. Thus, the pixel line to turn on can be shifted one by one, specifying the time amount which EL element 15 has turned on by scanning to one F/N. Thus, it is easy to realize to make the same the wave of gate signal line 17b, and to shift it in each pixel line. It is because what is necessary is just to control ST1 and ST2 which are data impressed to the shift registers 22a and 22b of drawing 2. For example, if Vgl is outputted to gate signal line 17b when an input ST 2 is L level, and Vgh is outputted to gate signal line 17b when an input ST 2 is H level, only the period of 1 F/N inputs ST2 impressed to shift register 17b on L level, and makes it H level at other periods. This inputted ST2 is only shifted with the clock CLK2 which synchronized with 1H.

[0390] Wave-like creation of gate signal line 17a similarly shown in drawing 33 (a) is also

easy. It is because what is necessary is just to control ST1 which is input data of shift register 22a of drawing 2. For example, if Vgl is outputted to gate signal line 17a when an input ST 1 is L level, and Vgh is outputted to gate signal line 17a when an input ST 1 is H level, only the period of 1H inputs ST1 impressed to shift register 17a on L level, and makes it H level at other periods. This inputted ST1 is only shifted with the clock CLK1 which synchronized with 1H.

[0391] Drawing 31 (b) is the example which moved two image display fields 311a and 311b to down from on the screen as the image display field 311 was made into 1/(2Ns) and was shown in an arrow head (drawing 31 (b1) -> drawing 31 (b2) -> drawing 31 (b3) -> drawing 31 (b1) ->). However, though migration of these image display fields 311a and 311b is not limited to moving to down from on the screen of a screen and moves to above from under a screen, it is good. Moreover, the 1st (1 field eye) frame is moved to down from on a screen, and it cannot be overemphasized that the following frame [2nd (2 field eye)] may be scanned so that it may move to above from under a screen (actuation). Moreover, you may scan from the right of a screen from the left or the left of a screen to the right (actuation). Moreover, this image display field 311a may be moved to down from on a screen, and image display field 311b may be moved to above from under a screen.

[0392] Furthermore, drawing 31 (c) is the example which moved three image display fields 311a and 311b to down from on the screen as the image display field 311 was made into 1/(3Ns) and was shown in an arrow head (drawing 31 (c1) -> drawing 31 (c2) -> drawing 31 (c3) -> drawing 31 (c1) ->).

[0393] As shown in drawing 31 (b) and (c), the more it divides the image display field 311 into plurality, the more the frame rate (a screen is rewritten in the count 60 which writes a screen in 1 second, for example, a frame rate, 60 times in 1 second) of the whole image display can be reduced. If a frame rate is reduced, since the part and the clock of a circuit of operation can be reduced, power consumption can be made small.

[0394] That is, the luminescence period of EL element 15 becomes short, and the instant brightness on appearance becomes high, and, moreover, for a ****** food **** reason, a flicker decreases [the image display field 311 and the astigmatism LGT field 312] at a high speed. Therefore, a frame rate can be reduced.

[0395] The count turned on in one frame (1 field) as mentioned above can be increased, and a flicker can be reduced. Since a frequency component becomes high in lighting of an EL element by increasing the count of lighting, human being's eyes become is hard to be observed. For example, when the lighting period per time is set to 1/7 and one frame was switched on 7 times, the display whose flicker frame frequency does not have in 30Hz was realizable.

[0396] The brightness of an image can be adjusted by controlling turning on and off of TFT11d (adjustable). For example, in the case of drawing 31 (a), the brightness of Screen 21 changes by changing the area of the astigmatism LGT field 312 (when the number of the image display fields 311 being one) (drawing 32 (a2) is darker than drawing 32 (a1), and drawing 32 (a3) is darker than drawing 32 (a2)).

[0397] Similarly, in the case of drawing 31 (b), drawing 32 (b2) is darker than drawing 32 (b1) (when the number of the image display fields 311 is two), and, in drawing 32 (b3), the display brightness of Screen 21 becomes dark from drawing 32 (b2). Moreover, the same is said of the case (3 or more [when the number of the image display fields 311 is three that is,]) of drawing 31 (c) (drawing 32 (c2) is darker than drawing 32 (c1), and drawing 32 (c3) becomes dark from drawing 32 (c2).).

[0398] In addition, although [the image display field 311] the Screen 21 top is scanned, an one-frame (1 field) eye makes a full screen the astigmatism LGT condition 312, and the following two-frame (2 field) eye is good [the field] in drawing 31, also considering a full

screen as an image display condition 311 so that it may not limit to this and may illustrate to drawing 32 (c1) (c2). That is, an image display condition and an astigmatism LGT condition are repeated for a full screen by turns. However, image display time amount and astigmatism LGT time amount are not limited to isochronous. For example, image display time amount is set to 1F/4, and it is good also considering astigmatism LGT time amount as 3F/4. Thus, the display brightness of an image can be changed also by changing the rate of image display time amount and astigmatism LGT time amount (adjustment).

[0399] Anyway, as shown in drawing 34, the display brightness B of an image can be changed to a linear by changing the value of N. Moreover, it can carry out adjustable [of the brightness of an image] easily only by controlling the value of N.

[0400] Drawing 35 is the block diagram of the circuit which adjusts the display brightness of this invention (control). The image data inputted from the outside are stored in a frame memory (field memory) 354. CPU353 calculates using the stored image data. An operation uses at least one or more of the maximum brightness of image data, optimal brightness, average luminance, and luminance distribution. Moreover, the maximum brightness, the optimal brightness, the average luminance, the luminance distribution, and its change rate of each frame of continuous image data are also taken into consideration.

[0401] The calculated result is stored in the brightness memory 352. The brightness memory 352 is data which amended the brightness of an image. For example, on bright screens, such as the seashore, when the average luminance of an image is amended brightly and there is a comparatively dark part within the image data, it changes into image data actually darker than a value. Moreover, on the screen of night, since it is dark on the whole, an image amends a comparatively bright part more brightly.

[0402] It is the circuit which counts how much a counter circuit 351 makes N-ary of drawing 34. In the wave of gate signal line 17b, N-ary is changed on real time. Since N-ary is time amount, by counting with a counter, it can be changed easily and can change the brightness of an image.

[0403] The change circuit 355 is a circuit which changes the electrical potential difference Vgl which makes TFT11 of a pixel 16 turn on, and the electrical potential difference Vgh (it is the reverse by N channel when the number of pixels TFT11 is P) made to turn off. That is, based on the output of a counter circuit 351, the period of 1 F/N shown in drawing 33 (b) is changed. Therefore, it can carry out adjustable [of the brightness of an image 21] easily on real time.

[0404] According to video-signal data, display brightness is controlled on real time. Thus, the dynamic range of a brightness expression is expandable to 3 or more times on parenchyma by controlling. Moreover, since EL display serves as a black display (astigmatism LGT) completely when not passing a current to EL, the black float of image display does not generate it, either. That is, contrast also becomes high. Especially in the case of a current program, to a black display, the current value programmed to a pixel is as small as 10nA(s). Therefore, it is difficult to be unable to carry out the charge and discharge of the parasitic capacitance 404 enough, but to realize a perfect black display. Moreover, power is supplied to the source signal line 18 by the pulse impressed to the gate signal line 17 (running electrical potential difference), and a black float is generated.

[0405] It suspends that this invention turns OFF TFT11d compulsorily, and supplies a current to EL element 15. Therefore, EL element 15 will be in an astigmatism LGT condition completely. Therefore, good contrast is realizable. Moreover, it is necessary to adjust the output timing of the data impressed to the source signal line 18, and the timing of the gate signal lines 17a and 17b. As for especially the output of Vgl (electrical potential difference which makes TFT(s) 11b and 11c of drawing 1 turn on) of gate signal line 17a which chooses a pixel line, it is more desirable than 1H to make it become short. Drawing 252 also explains

this.

[0406] In addition, in drawing 35, based on the image data of a video signal although the brightness of an image is changed on real time, it does not limit to this. For example, a user's pushing a brightness adjustment switch or a brightness adjusting volume is turned. This change may be detected, adjustable [of the counter value of a counter circuit 351] may be carried out, and the brightness (or contrast or a dynamic range) of a display image 21 may be changed. Moreover, a phot sensor may detect brightness, such as outdoor daylight, and the brightness of a display image 21 etc. may be automatically changed based on this detected data. Moreover, you may constitute so that it may be manual or may be made to change with the contents of the image to display, and data automatically.

[0407] Brightness adjustment is realizable by making TFT by the side of EL element 15 (drawing 1 TFT11d) turn on and off. In this case, the program current (electrical potential difference: in the case of an electrical-potential-difference program method) outputted from a source drive IC 14 is a fixed value (a program current is not changed). Therefore, the circuitry of the source driver IC can be simplified. That is, it is not necessary to change the output current (electrical potential difference) etc. corresponding to the brightness of the display screen. For example, by the conventional liquid crystal display panel, 64 gradation eye of the maximum brightness is used at the time of 64 gradation displays. From this, when lowering brightness by brightness adjustment, the period until 32 gradation eye is used. Thus, if a circuit is constituted, when screen intensity is dark, the number of gradation displays will decrease.

[0408] However, by the method made to turn on and off TFT11 by the side of EL element 15 (the current which flows to EL element 15 is indicated by intermittent), adjustment of a "off" period can adjust brightness freely. In that case, even if the brightness adjustment by this invention changes gamma adjustment and linearity changes brightness, it can hold. Since supply voltage Vdd is also a fixed value, a configuration top is also advantageous.

[0409] Moreover, the Gaussian distribution of the brightness of a screen can be easily carried out by controlling an on-off condition to become Gaussian distribution from on a screen about TFT11d down. Most control has an unnecessary operation. Forge-fire [back] explanation is given about this approach.

[0410] In addition, it is necessary to set to 0.5 or more msecs the period which turns EL element 15 on and off. When this period was short, it will not be in a perfect black display condition with the after-image property of human being's eyes, but an image came to have faded, and resolution came to have fallen. Moreover, it will be in the display condition of the display panel of a data-hold mold. However, when an on-off period is set to 100 or more msecs, it is visible to a flashing condition. Therefore, the on-off period of an EL element should be made 100 or less msec more than 0.5microsec. The on-off period should be made still more preferably 2 or more-msec 30 or less msec. The on-off period should be made still more preferably 3 or more-msec 20 or less msec.

[0411] Although the number of partitions of the black screen 1312 can realize a good movie display if it is set to one, a flicker of a screen becomes easy to be in sight. Therefore, it is desirable to divide the black insertion section into plurality. However, if the number of partitions is made [many / too much], animation dotage will occur. The number of partitions should carry out to eight or less [1 or more]. It is desirable to carry out to five or less [1 or more] still more preferably.

[0412] In addition, as for the number of partitions of a black screen, it is desirable to constitute so that it can change by the still picture and the animation. In N= 4, 75% is a black screen and 25% of the number of partitions is image display. At this time, the number of partitions 1 scans 75% of black display in the vertical direction of a screen in the state of 75% of black obi. It is the number of partitions 3 which is scanned by 3 blocks of 25% of black

screen, and 25/3% of display screen. A still picture makes [many] the number of partitions. An animation lessens the number of partitions. a change -- an input image -- responding -- being automatic (animation detection etc.) -- you may carry out and a user may carry out manually. Moreover, what is necessary is just to constitute so that it can change to the image of a display etc. and may be made it corresponding to an input plug socket.

[0413] For example, in a cellular phone etc., the number of partitions is made or more into ten by a wallpaper display and the input screen (you may turn on and off to every 1H extremely). When displaying the animation of NTSC, the number of partitions is made or less [1 or more] into five. In addition, as for the number of partitions, it is desirable to constitute so that it can change to three or more multistage stories. For example, it is number-of-partitions nothing, 2, 4, 8, etc.

[0414] Moreover, when area of a full screen is set to 1, as for the rate of a black screen to all the display screens, it is desirable to carry out to 0.9 (for it to be nine or less [1.2 or more], if it displays by N) or less [0.2 or more]. Moreover, it is desirable to carry out to 0.6 (for it to be six or less [1.25 or more], if it displays by N) especially or less [0.25 or more]. The improvement effect in a movie display is low in it being 0.20 or less. The brightness for a display becomes it high that it is 0.9 or more, and it becomes that the amount of display moves up and down that it is easy to be recognized visually.

[0415] Moreover, as for the frame number per second, 100 (10Hz or more 100Hz or less) or less [10 or more] are desirable. 65 (12Hz or more 65Hz or less) or less [further 12 or more] are desirable. When there are few frame numbers, a flicker of a screen comes to be conspicuous, if there are too many frame numbers, the writing from a driver circuit 14 etc. will become painful, and resolution will deteriorate.

[0416] Anyway, in this invention, the brightness of an image can be changed by control of the gate signal line 17. However, it cannot be overemphasized that you may carry out by the brightness of an image changing the current (electrical potential difference) impressed to the source signal line 18. Moreover, it cannot be overemphasized that you may carry out combining control of the gate signal (using drawing 33, drawing 35, etc.) line 17 explained previously and changing the current (electrical potential difference) impressed to the source signal line 18.

[0417] In addition, it cannot be overemphasized that the above matter can also apply the pixel configuration of electrical-potential-difference programs, such as drawing 54, drawing 67, and drawing 103. For example, what is necessary is just to carry out on-off control of the TFT11e in drawing 67.

[0418] The time of day which sets only the period of 1 F/N of gate signal line 17b to Vgl is 1F (it does not limit to 1F.) so that it may illustrate to drawing 36. It is good at a unit period. Any time of day is sufficient among periods. When only a predetermined period makes unit time amount turn on EL element 15 inside, it is because it is what obtains predetermined average luminance. Set gate signal line 17b to Vgl immediately, and make it however, better for EL element 15 to emit light in the program period (1H) of drawing 36 (a). It is because it is hard coming to win popularity the effect of the retention property of the capacitor 19 of drawing 1. Moreover, in drawing 36 (b), as the notation and arrow head of A and B show, the period of one F/N may be constituted so that a location may be changed. This change is also easily realizable. the timing (when [of 1F] is it made L level?) of the data impressed to ST in drawing 2 -- adjustment -- or it is because what is necessary is just to constitute so that it can carry out adjustable.

[0419] Moreover, the period (1 F/N) which sets gate signal line 17b to Vgl may be divided into plurality so that it may illustrate to drawing 37 (number of partitions K). That is, the period set to Vgl carries out the period of 1F/(K/N) K times. Thus, if it controls, an image display condition will become about drawing 31 (b), (K= 2), and drawing 31 (c) and (K= 3).

Thus, by dividing into plurality the image section (image display section 311) made to turn on, generating of a flicker can be controlled and image display of a low frame rate can be realized. Moreover, it is desirable to constitute so that it can carry out adjustable [of the number of partitions of this image]. For example, that a user pushes a brightness adjustment switch or by turning a brightness adjusting volume, this change is detected and the value of K is changed. You may constitute so that it may be manual or may be made to change with the contents of the image to display, and data automatically.

[0420] Thus, it is also easily realizable to change the value (number of partitions of the image display section 311) of K. the timing (when [of 1F] is it made L level?) of the data impressed to ST in drawing 2 -- adjustment -- or it is because what is necessary is just to constitute so that it can carry out adjustable.

[0421] In addition, in drawing 37, the period (1 F/N) which sets gate signal line 17b to Vgl is divided into plurality (number of partitions K), and although [the period set to Vgl] the period of 1F/(K/N) is carried out K times, it is not this-limited. L (L!=K) time operation of the period of 1F/(K/N) may be carried out. That is, this invention displays an image 21 by controlling the period (time amount) passed to EL element 15. Therefore, carrying out L (L!=K) time operation of the period of 1F/(K/N) is included in the technical thought of this invention. Moreover, the brightness of an image 21 can be changed in digital one by changing the value of L. For example, by L= 3, 50% of brightness (contrast) change is set to L= 2. These control is also easily realizable by circuitry, such as drawing 2, drawing 35, drawing 60, and drawing 74.

[0422] Moreover, when dividing the viewing area 311 of an image, the period which sets gate signal line 17b to Vgl is not limited to the same period. For example, the period set to Vgl as shown in drawing 38 is good also as two or more periods like t1 and t2.

[0423] The above example was what turns the display screen 21 on and off (lighting, astigmatism LGT) by connecting the current which intercepts the current which flows to EL element 15, and flows to an EL element. That is, multiple times and an abbreviation same current are passed to TFT11a with the charge held at the capacitor 19. This invention is not limited to this. For example, the method which turns the display screen 21 on and off (lighting, astigmatism LGT) may be used by carrying out the charge and discharge of the charge held at the capacitor 19.

[0424] Drawing 303 is the example. In the pixel configuration of drawing 1, TFT11e which carries out a switching element is arranged or formed in the both ends of a capacitor 19. By impressing ON state voltage (Vgl) to gate signal line 17e connected to the gate terminal of TFT11e, TFT11e turns on and the both ends of a capacitor 19 are short-circuited. Vg electrical potential difference turns into a Vdd electrical potential difference, and it becomes impossible therefore, to pass TFT11a with a current.

[0425] Of course, a switching element is arranged or formed between the (Drain D)-(gate G) terminals of TFT11a, and even if it short-circuits between the (Drain D)-(gate G) terminals of TFT11a, TFT11a can be prevented from passing a current. Therefore, it cannot be overemphasized that this configuration may be used. For example, it is the configuration of constituting so that the gate terminal of TFT11b of drawing 1 and the gate terminal of TFT11c can be controlled according to an individual, making TFT11b turning on, and short-circuiting between the (Drain D)-(gate G) terminals of TFT11a. This method is applicable also to drawing 21, drawing 43, drawing 71, and drawing 22. In drawing 21, drawing 43, drawing 71, and drawing 22, it is the configuration of impressing ON state voltage (Vgh) to gate signal line 17b, making TFT11d turning on, and short-circuiting between the (Drain D)-(gate G) terminals of TFT11a.

[0426] Of course, it cannot be overemphasized that the above configurations (the method to which the charge and discharge of the maintenance charge of TFT11 for a drive are carried

out, method which short-circuits between the (Drain D)-(gate G) terminals) are applicable also to the pixel configuration of electrical-potential-difference drives, such as drawing 54, drawing 67, drawing 68, and drawing 103.

[0427] In addition, TFT11e is not limited to switching elements, such as TFT. what can carry out the charge and discharge of the charge of the both ends of a capacitor 19 -- be -- what can creep may be used. For example, MIM, TFD (thin-film diode), a thyristor, a varistor, etc. are sufficient. Moreover, not the thing that limits the both ends of a capacitor 19 to what carries out charge and discharge but the thing which can shift compulsorily the terminal voltage Vg of the component for a drive which passes a current to EL element 15 in the current off direction may be used. For example, you may constitute so that it may run and Vg electrical potential difference can be shifted with an electrical potential difference using a capacitor etc.

[0428] With the configuration of drawing 303, since the charge of a capacitor 19 is discharged by actuation of TFT11e, a current cannot be again passed to EL element 15. However, the brilliance control of the display screen 21 can be easily carried out from that of controlling a time interval until it makes TFT11e turn on (adjustment). Moreover, color adjustment of the display screen 21 can be easily carried out from that of controlling a time interval until it makes every R, G, and B turn on TFT11e (adjustment). It cannot be overemphasized that the configuration of drawing 303 is combinable with other examples given [, such as N double pulse drive of reverse bias voltage system, drawing 87, etc. and a Gaussian distribution drive, and a block drive, / this] in a specification. Moreover, since other configurations and actuation have already explained, they are omitted. The above matter is the same also about other this inventions.

[0429] Moreover, in drawing 303, it was the method which intercepts the current which flows to TFT11a by making TFT11e turn on. However, it is also possible by using TFT11a as N channel etc. to control to make the current which flows to TFT11a for a drive increase. That is, when TFT11e operates, it can be said that Screen 21 makes it a white display (white raster) (a screen is eliminated on a white screen). moreover, the pixel of RGB -- inside, when TFT11e of at least 1 color operates, it can be said that Screen 21 makes it R, G, or a B display (R, G, or B color is strongly displayed for a screen). In addition, it cannot be overemphasized that P channels or N channel is sufficient as TFT11e. Moreover, an PWM modulation can also be carried out by making TFT11e turn on and off. It cannot be overemphasized that the above matter is applicable to other examples of this specification.

[0430] Drawing 303 configuration is a method which discharges the charge of a capacitor 19 completely. Therefore, the charge (image data) held at the capacitor 19 will be eliminated. The configuration of drawing 304 divided the capacitor 19 into the capacitors 19a and 19b of plurality (an example two), and forms or arranges TFT11e to the both ends of one capacitor (an example 19b).

[0431] Drawing 304 is the example. By impressing ON state voltage (Vgl) to gate signal line 17e connected to the gate terminal of TFT11e, TFT11e turns on and the both ends of capacitor 19b are short-circuited. Therefore, Vg electrical potential difference becomes more close to a Vdd electrical potential difference, and lessens the current which TFT11a passes (it restricts).

[0432] Therefore, with the configuration of drawing 304, the current which TFT11a passes is not intercepted completely (the constant of Capacitors 19a and 19b can be set up so that it may intercept completely, of course). With the configuration of drawing 303, since the charge of a capacitor 19 is discharged by actuation of TFT11e, a current cannot be again passed to EL element 15. However, if TFT11e is turned off, although display brightness is lower than before, an image can be again expressed as the configuration of drawing 304. moreover, that of controlling a time interval until it makes TFT11e turn on (adjustment) -- the brilliance control of the display screen 21 -- texture -- it can carry out to adjustment (modification)

warm.

[0433] Moreover, even if it is in a solid-state difference for every panel (when manufacture variation occurs etc.), the variation in display brightness can be adjusted by making TFTe make turn on or turn off for every manufactured display panel. In this case, TFT11e always has ON or the case of being off. Moreover, from that of controlling a time interval until it makes every R, G, and B turn on TFT11e (adjustment), it opts for color adjustment of the display screen 21, and adjusts easily warm. What is necessary is just to adopt the configuration explained as a pixel configuration in drawing 294 etc. Moreover, it cannot be overemphasized that it is combinable with other examples given in a book specification, such as reverse bias voltage system, also about the configuration of drawing 304 etc. Moreover, since other configurations and actuation have already explained, they are omitted. The above matter is the same also about other this inventions.

[0434] In addition, in drawing 304, although carried out to two of Capacitors 19a and 19b, it does not limit to this. Three or more capacitors may be formed, and switching elements, such as TFT, may be arranged so that the charge and discharge of the charge of each capacitor can be carried out. In this configuration, the brightness of the display screen 21 can be changed in other phases. Moreover, color balance of RGB can also be adjusted on a multistage story (modification).

[0435] Moreover, in drawing 304, it was the method which decreases the current which flows to TFT11a by making TFT11e turn on. However, it is also possible by using TFT11a as N channel etc. to control to make the current which flows to TFT11a for a drive increase. That is, when TFT11e operates, the brightness of Screen 21 can be made high. moreover, the pixel of RGB -- R, G, or B color can be made to increase the color of Screen 21, when TFT11e of at least 1 color operates inside (R, G, or B color is strongly displayed for a screen.) In addition, there is also a case of two or more colors like R and B.

[0436] Moreover, although it was the configuration in which one capacitor 19a was formed between the gate (G) terminal of TFT11a, and (Source S) terminal, in drawing 304, it does not limit to this. The configuration which formed two or more capacitor 19a between the gate (G) terminal of TFT11a and (Source S) terminal at a serial or juxtaposition may be used. The current which flows to TFT11a may be decreased by forming switching TFT11e for short in the both ends of at least one capacitor among this capacitor, and making TFT11e turn on. It cannot be overemphasized that the above matter is applied also to the pixel configuration of a current mirror or the pixel configuration of an electrical-potential-difference drive.

[0437] Drawing 305 is the configuration in which TFT11e which short-circuits the both ends of the capacitor 19 for maintenance was formed (arrangement), in the pixel configuration of the current mirror explained by drawing 21, drawing 43, drawing 71, etc. Since actuation etc. is the same as that of drawing 303 etc., explanation is omitted. The same is said of drawing 305. Since actuation etc. can be easily guessed from explanation or explanation of drawing 304 in drawing 304, explanation is omitted.

[0438] Drawing 307 is the example of an electrical-potential-difference drive of a pixel of 2TFT configurations. The current drive method and actuation which also explained the configuration of drawing 307 in drawing 303 etc. are the same. TFT11e is formed in the both ends of the capacitor 19 for maintenance (arrangement). Like the configuration previously explained also with the configuration of drawing 307, since the charge of a capacitor 19 is discharged by actuation of TFT11e, a current cannot be again passed to EL element 15. However, the brilliance control of the display screen 21 can be easily carried out from that of controlling a time interval until it makes TFT11e turn on (adjustment). Moreover, color adjustment of the display screen 21 can be easily carried out from that of controlling a time interval until it makes every R, G, and B turn on TFT11e (adjustment).

[0439] Moreover, it is also possible also about the configuration of drawing 307 to control to

make the current which flows to TFT11a for a drive increase by making TFT11e turn on by using TFT11a as N channel etc. That is, when TFT11e operates, it can be said that Screen 21 makes it a white display (white raster) (a screen is eliminated on a white screen). moreover, the pixel of RGB -- inside, when TFT11e of at least 1 color operates, it can also be said that Screen 21 makes it R, G, or a B display (R, G, or B color is strongly displayed for a screen).

[0440] Drawing 308 is drawing 67 and the example which applied the technical concept of drawing 303 to the pixel configuration of the electrical-potential-difference program (drive) of drawing 68. The current drive method and actuation which also explained the configuration of drawing 308 in drawing 303 etc. are the same. That is, TFT11e is formed in the both ends of the capacitor 19 for maintenance, and the charge of a capacitor 19 is discharged by actuation of TFT11e. Therefore, it becomes a black display. Color adjustment of the display screen 21 can be easily carried out from that of controlling a time interval until it can carry out the brilliance control of the display screen 21 easily and makes every R, G, and B turn on TFT11e from that of controlling a time interval until it makes TFT11e turn on (adjustment) (adjustment). Since it is the same as that of a previous example about other matters, explanation is omitted.

[0441] Although it illustrated in drawing 33 so that sequential lighting (display) of the adjoining pixel line might be carried out, this invention is not limited to this. Interlace scanning may be carried out so that it may illustrate to drawing 39.

[0442] Interlace scanning writes an image in an odd-pixel line (drawing 39 (a) write-in pixel line 391), writes an image in an even-pixel line in the 2nd next field (drawing 39 (b) write-in pixel line 391), and is the image display approach in the 1st field. The pixel line which is not written in holds the image data of the front field (maintenance pixel line 392). Thus, a flicker can be decreased by carrying out interlace scanning with EL display.

[0443] In the drive of drawing 39, gate signal line 17b of all even-pixel lines (or plurality) is made in common, and gate signal line 17b of all odd-pixel lines (or plurality) is made in common. Therefore, the number of leading about of the gate signal line 17 is sharply reducible. Moreover, when displaying the display condition 311 and the non-display condition 312 for a full screen by turns, all gate signal line 17b is made in common. These configurations are effective with especially configurations free three sides, such as drawing 27.

[0444] In addition, although [interlace scanning / in the 1st field] an image is written in an odd-pixel line and an image is written in an even-pixel line in the 2nd next field, it is not limited to this. the 1st field -- a 2-pixel line -- it may fly and come out, and you may write in a 2-pixel line [every] image, and may also write in an image for every 2-pixel line which was not written in in the 1st field in the 2nd next field. moreover, every [every / a 3 pixel line / or / a 4 pixel line] are sufficient. moreover, in the 1st field, you may write in the 2-pixel line [every] image of a screen from the 2nd line (see the drawing 106 (a)), and may also write in an image for every 2-pixel line from the 1st line in the 2nd next field (see the drawing 106 (b)). Moreover, the pixel line or the pixel line to write in currently written in so that it may illustrate to drawing 106 may be controlled to become the non-display field 312. Moreover, in the 1st field, you may write in an image toward the bottom from on a screen, and may also write in an image toward a top from under a screen in the 2nd field. These are also all contained in the concept of interlace scanning.

[0445] Interlace scanning is also easily realizable by enforcing the approach explained by drawing 33 and drawing 56. It is because the pixel line applicable to the viewing area 312 which is not made to turn on should just make TFT11d shown in drawing 1 (a) turn off.

[0446] Moreover, the black viewing area 312 and interlace scanning are combinable so that it may illustrate to drawing 50 with a natural thing. In drawing 50 (a), the sequential shift of the scan field 501 which consists of a write-in pixel line 391 and a maintenance pixel line 392 is

carried out. In addition, in drawing 50 (a), the image is written in from the 1st line. Drawing 50 (b) carries out the sequential shift of the scan field 501 which consists of a write-in pixel line 391 and a maintenance pixel line 392 similarly. In addition, in drawing 50 (b), the image is written in from the 2nd line.

[0447] If interlaced scanning (interlace scanning etc.) is applied, the variation in the drive TFT11 of a pixel 16 will be controlled, and the thing of it can be carried out. Drive TFTT11a of the adjoining pixel line approaches, and drawing 322 is formed (arrangement). That is, TFT 11a1 of pixel 16a and TFT 11a2 of pixel 16b approach, and are arranged. Moreover, the gate signal line 17a1 which controls pixel 16a, and the gate signal line 17a2 which controls pixel 16b also approach, and is arranged. The gate signal line 17a1 and the gate signal line 17a2 approach, and are arranged for considering pixel 16a and pixel 16b as arrangement of axial symmetry.

[0448] TFT 11a2 and the property of TFT11a1 approximate by approaching and arranging TFT 11a1 of the pixel line containing pixel 16a, and TFT 11a2 of the pixel line containing pixel 16b, as shown in drawing 322. Hereafter, the drive approach using the pixel arrangement configuration of drawing 320 is explained using drawing 323 and drawing 324.

[0449] Drawing 323 is an explanatory view of other examples which increase the current which flows to the source signal line 18. It is the method which chooses a 2-pixel line as coincidence, carries out the charge and discharge of the parasitic capacitance 404 of the source signal line 18 etc. with the current with which the 2-pixel line was united, and improves current write-in lack sharply. However, since a 2-pixel line is chosen as coincidence, one half of the currents (program current) which pass the current which per pixel drives to the source signal line 18 can be decreased. Therefore, since the current which flows to EL element 15 can be decreased, there is little degradation of EL element 15. Here, in order to give explanation easy, it explains as N= 2 as an example (the current passed to a source signal line is doubled). In addition, drawing 87, drawing 88, etc. explain the similar drive approach. Therefore, please also refer to these approaches.

[0450] Drawing 323 (a) is illustrating the write-in condition to a display image 21. In drawing 323 (a), 871 (871a, 871b) is a write-in pixel line. That is, 2 pixels is written in. The twice as many program current Iw as the current written in a pixel is impressed to the source signal line 18. Therefore, since there are two pixel lines, the current written in 1 pixel becomes 1 time (predetermined value). As for the condition of drawing 323 (a), 1-pixel line selection of pixel 16a and the pixel 16b will be made, respectively. That is, the current program will be carried out as operated in the drive TFT 11a1 of the pixel which approached, and 11a2 (the pixel configuration of drawing 1 is assumed). The current Iw passed to the source signal line 18 is supplied from this TFT 11a1 for a drive arranged by approaching, and TFT 11a2 for a drive.

[0451] Since TFT 11a1 for a drive and TFT 11a2 for a drive approach and are formed, the property's correspond mostly. Therefore, as for 2 (muA), then TFT 11a1 for a drive and TFT 11a2 for a drive, the program current Iw which flows to the source signal line 18 supplies 1 (muA) every current, respectively.

[0452] From the above thing, if the twice as many program current Iw as a predetermined value is passed to the source signal line 18, the current of a predetermined value will be correctly programmed by the pixel. In addition, although the current passed to the source signal line 18 was made into twice (N= 2), it is not limited to this. It could be twice for making an understanding easy to the last. In the real drive, in order to carry out one half of screen products, the program current makes the astigmatism LGT field 312 4 times.

[0453] In the pixel configuration of drawing 322, one screen is rewritten in the 2 field (one frame = 2 field). Even lines is rewritten, and the 1st field explains in the 2nd field noting that odd lines is rewritten. It explains rewriting even lines, and drawing 323 explains in drawing

324 noting that odd lines is rewritten.

[0454] In drawing 323, 871 (871a, 871b) is a write-in pixel line, and is writing in 2 pixels. The twice as many program current Iw as the current written in odd pixels is impressed to the source signal line 18. Therefore, the write-in pixel lines 871a and 871b serve as the same display. Then, EL element 15 of the pixel which corresponds to odd lines so that it may illustrate to drawing 323 (b) is made into an astigmatism LGT condition (OFF state voltage is impressed to gate signal line 17b, and it is made for the current from TFT11a for a drive not to flow to EL element 15 in drawing 1). image data is written in the pixel, shifting the above actuation a 2-pixel number every. After the scan of the 1 field is completed, it becomes astigmatism LGT 312 and all [of even lines] odd lines become lighting 311 so that it may illustrate to drawing 323 (c).

[0455] Drawing 324 is illustrating the image data write-in condition of the 2nd field. In drawing 324 (a), 871 (871a, 871b) is a write-in pixel line, and is writing in 2 pixels. The twice as many program current Iw as the current written in odd pixels is impressed to the source signal line 18. Therefore, the write-in pixel lines 871a and 871b serve as the same display. EL element 15 of the pixel which corresponds to even lines so that it may illustrate to drawing 324 (b) like the 1st field is made into an astigmatism LGT condition. image data is written in the pixel, shifting the above actuation a 2-pixel number every. After the scan of the 1 field is completed, it becomes astigmatism LGT 312 and all [of odd lines] (odd-numbered pixel line) even lines (even-numbered pixel line) become lighting 311 so that it may illustrate to drawing 324 (c).

[0456] As mentioned above, one screen is rewritten by one frame (2 field) by repeating the drive of drawing 323 and drawing 324 by turns. Moreover, as shown in drawing 322, by making a 2-pixel line into a pair, TFT11a for a drive of a 2-pixel line was made to approach, and it has controlled that property variation occurs. Therefore, uniform image display is realizable.

[0457] In addition, pixel arrangement of drawing 322 and the drive approach are not limited only to the pixel configuration of drawing 1. For example, it cannot be overemphasized that it is applicable also to the pixel configuration of electrical-potential-difference program methods, such as a pixel configuration of drawing 21, drawing 43, drawing 71, and the current mirror of drawing 22, drawing 54, drawing 67, drawing 68, and drawing 103.

[0458] With the pixel configuration of drawing 21, drawing 43, and drawing 71, the current value impressed to the source signal line 18 is programmed by the capacitor 19 by impressing ON state voltage (Vgl) to gate signal line 17a. The data which correspond to a video signal from the current source 403 in the source driver IC 14 are impressed to the source signal line 18 so that it may illustrate to drawing 40. When current mirror effectiveness is 1, said current flows to TFT11b and, as for the programmed current, this current is impressed to EL element 15. Probably, **** does not have these relation (timing wave etc.) in explanation, since it can divert the matter illustrated to drawing 33 or is similar. However, in case a current program is performed, it may be necessary to control ON or off timing of TFT11c and TFT11d according to an individual. In this case, it cannot be overemphasized that it is necessary to make into another gate signal line 17 the gate terminal made to turn TFT11c and TFT11d on and off.

[0459] In order to enforce the methods of presentation, such as drawing 31, it is necessary to intercept the current passed to EL element 15. TFT11e is added so that it may illustrate to drawing 40 for the purpose of this cutoff. By setting the gate terminal of TFT11e to Vgl, a current is impressed to EL element 15 and the current to EL element 15 will be in a cutoff (astigmatism LGT condition) condition by setting the gate terminal of TFT11e to Vgh.

[0460] Therefore, the image display explained by drawing 31 etc. is realizable by impressing the signal wave form of the gate signal lines 17a and 17b explained by drawing 33 etc.

[0461] The non-image display field 311 and the image display field 312 may change an odd-pixel line and an even-pixel line to every frame (field) so that it may illustrate to drawing 61. Drawing 61 (a) displays an odd-pixel line, and by non-display, then following FIMU (field) (see drawing 61 (b)), an odd-pixel line is made a non-example and it makes an even-pixel line a display for an even-pixel line.

[0462] Thus, if it displays that a non-display field and a viewing area are repeated for every 1-pixel line, generating of a flicker will be controlled sharply.

[0463] In addition, in drawing 61, although it is made a non-display pixel line and a display pixel line for every 1-pixel line, though it does not limit to this and is made a non-display pixel line and a display pixel line for every pixel line beyond every 2-pixel line and it, it is good.

[0464] For example, if it is every two lines, in the 1st field (frame), eye a 1-pixel line and eye a 2-pixel line will consider as a display pixel line, and will make eye a 3-pixel line and eye a 4-pixel line a non-display pixel line. Eye a 5-pixel line and eye a 6-pixel line are display pixel lines. In the 2nd next field (frame) of the 1st field, eye a 1-pixel line and eye a 2-pixel line consider as a non-display pixel line, and make eye a 3-pixel line and eye a 4-pixel line a display pixel line. Eye a 5-pixel line and eye a 6-pixel line are non-display pixel lines. Moreover, in the 3rd next field (frame), eye a 1-pixel line and eye a 2-pixel line consider as a display pixel line, and make eye a 3-pixel line and eye a 4-pixel line a non-display pixel line. Eye a 5-pixel line and eye a 6-pixel line are display pixel lines.

[0465] In addition, **** of the field and a frame is used for homonymy, or this specification has separated it. Generally one frame consists of interlace drives of NTSC in the 2 fields. However, in a progressive drive, one frame is the 1 field. Thus, in the world of the signal of an image, the field and a frame are used properly. However, in this invention, the image displayed on a display panel can apply progressive, an interlace, or either. Therefore, it is considering as the expression that whichever is sufficient. It is the unit of the time amount to which one finishes writing a screen notionally also with the field or a frame.

[0466] The method of presentation of drawing 62 is also effective. In order to give explanation easy here, the 2nd field (the 2nd frame) and drawing 62 (c) consider as the 3rd field (the 3rd frame), and drawing 62 (d) considers [drawing 62 (a) / the 1st field (the 1st frame) and drawing 62 (b)] as the 4th field (the 4th frame).

[0467] In the 1st field (frame), eye a 1-pixel line and eye a 2-pixel line consider as a non-display pixel line, and make eye a 3-pixel line and eye a 4-pixel line a display pixel line. Eye a 5-pixel line and eye a 6-pixel line are display pixel lines. In the 2nd field (frame), eye an odd-pixel line considers as a display pixel line, and makes eye an even-pixel line a non-display pixel line. In the 3rd field (frame), eye a 1-pixel line and eye a 2-pixel line consider as a display pixel line, and make eye a 3-pixel line and eye a 4-pixel line a non-display pixel line. In the 4th field (frame), eye an odd-pixel line considers as a non-display pixel line, and makes eye an even-pixel line a display pixel line. Henceforth, it repeats successively from the display condition of the 1st field (the 1st frame).

[0468] By the drive approach of drawing 62, it is considering as one loop formation in the 4 field (frame). Thus, by performing image display in two or more fields (multiple frame), generating of a flicker is controlled rather than drawing 61 in many cases.

[0469] In addition, in the example of drawing 62, in the 1st field (frame), it considers as a 2-pixel line [every] non-display pixel line, and although considered as the 1-pixel line [every] non-display pixel line, it does not limit to this in the 2nd field (frame). In the 1st field (frame), it considers as a 2-pixel line [every] non-display pixel line, and although considered as the 1-pixel line [every] non-display pixel line, it does not limit to this in the 2nd field (frame). In the 1st field (frame), it considers as a 4-pixel line [every] non-display pixel line. In the 2nd field (frame) It considers as a 2-pixel line [every] non-display pixel

line. In the 3rd field (frame) It considers as a 1-pixel line [every] non-display pixel line, considers as a 4-pixel line [every] non-display pixel line in the 4th field (frame), considers as a 2-pixel line [every] non-display pixel line in the 5th field (frame), and is good also as a pixel line [every] non-display pixel line in the 6th field (frame).

[0470] The drive approach of this invention is easy to realize the display effectiveness (the animation effectiveness etc.). Drawing 63 is the method of presentation with which a viewing area appears one by one with drawing 63 (a) -> drawing 63 (b) -> drawing 63 (c) -> drawing 63 (d). The animation effectiveness is realizable by scrolling the non-display field 312 slowly. These control is also easily realizable by circuitry, such as drawing 2, drawing 60, and drawing 74. That is, a black display condition is not written in as an image, but control of gate signal line 17b etc. can realize the animation effectiveness easily.

[0471] The display panel which holds 1 field (one frame) period data to pixels, such as a liquid crystal display panel, has the technical problem that animation dotage occurs. Since CRT etc. is only displayed with an electron gun for a moment, the problem of animation dotage is not generated.

[0472] An effective means is black insertion solving this technical problem. This invention can realize easily the black insertion method which carries out near to CRT which reached to an extreme of a movie display.

[0473] Drawing 64 shows the place where the alphabetic character F moves downward from on a screen. However, the alphabetic character was set to F for making a plot easy. The non-display condition (drawing 64 (b), (d), (f)) is inserted between image display (drawing 64 (a), (c), (e)) so that it may illustrate to drawing 64. Therefore, an image serves as a discontinuous display. The sake. Animation dotage does not occur but a good movie display can be realized.

[0474] What is necessary is just to adopt the circuitry of drawing 60 as this business, for making a full screen into a non-display field. The difference with drawing 2 is the point of providing the ENBL terminal 601. The ENBL terminal 601 is connected to the end child of OR circuit 602 in which the gate signal line 17 was formed. By making an ENBL terminal into L level, Vgh level will be outputted to all gate signal line 17b, TFT 11d or 11e which supplies a current to EL element 15 will be in an OFF state, and a full screen serves as the non-display field 312. Normal operation is carried out when an ENBL terminal is H level.

[0475] In addition, although drawing 2, drawing 60, drawing 74, and drawing 84 explained the data inputted into ST terminal as carrying out the sequential shift with the clock (serial actuation), it does not limit to this. For example, you may be the parallel input which determines the on-off condition of each gate signal line at once (the ONFUFU logic of all gate signal lines corresponds [a part for the number of a controller or the gate signal line 17, the configuration for which are outputted at once and it opts]).

[0476] Although the example of drawing 64 was animation display, operation of the animation effectiveness, such as carrying out flash plate INGU, is also easy for every R, G, and B (refer to drawing 65). In drawing 65, drawing 65 (a) is [the image of green display 311G and drawing 65 (c) of the image of red display 311R and drawing 65 (b)] the images of blue display 311B. The image of red display 311R of drawing 65 (a) and drawing 65 (b) insert the image of green display 311G between each of the image of blue display 311B, and drawing 65 (c) is inserting the non-display condition (drawing 65 (b), (d), (f)). This actuation can be displayed that the image of R, G, and B is carrying out flash plate INGU if drawing 65 (f) is slowly carried out from drawing 65 (a).

[0477] an image which is different although the example of drawing 64 was animation display -- ** -- operation of the animation effectiveness, such as it being alike and carrying out flash plate INGU, is also easy (refer to drawing 66). In drawing 66, drawing 66 (a) is [2nd image 311b and drawing 66 (c) of 1st image 311a and drawing 66 (b)] 3rd image 311B. Drawing 66 (a) is inserting the non-display condition (drawing 66 (b), (d), (f)) between each

of 1st image 311a, 2nd image 311b of drawing 66 (b), and 3rd image 311B of drawing 66 (c). This actuation can be displayed that the 1st, 2nd, and 3rd image is carrying out flash plate INGU if drawing 66 (f) is slowly carried out from drawing 66 (a).

[0478] the above example was the approach (configuration) of only the period of 1-/N passing a twice [N] as many current as this for a twice [N] as many current as this to a predetermined value at a sink and EL element 15 to the source signal line 18 notionally, and obtaining desired brightness. By this approach (configuration), the technical problem of a write-in contingency by existence of parasitic capacitance 404 was solved.

[0479] In addition, luminous efficiency of the drive approach to N Double improves rather than 1 time (the conventional drive method). TFT11b (capacitor 19 side) of drawing 1 runs through this, and it is the effect of an electrical potential difference. the direction N doubled -- this -- it runs and the effect of an electrical potential difference can be mitigated. 1.5 or more-time 8 or less times are suitable for N multiple. Since the luminous efficiency of EL falls that it is more than this, effectiveness falls as a whole. Preferably, 6 or less twice [more than] as many times of N times as this are desirable. Moreover, I hear that a luminescence period is carried out to N Doubling at 1-/N, and it is. It will be said that it is desirable to carry out and to carry out a luminescence period to N making backlash 6 or less times more than twice 1/6 or less [1/2 or more] (at the time of the usual brightness).

[0480] In addition, after this invention makes TFT11d turn off and intercepts the current to EL element 15, it can pass a current like the point to EL element 15 by making TFT11d turn on again. This invention applied this principle well, for example, has acquired the current for a sink and predetermined brightness at the period of 1-/N. Thus, it can drive because the current value to pass is held every pixel 16 at the capacitor 19. That is, this invention can say that the characteristic pixel configuration of EL display panel has applied well, if the current value passed to EL element 15 is held.

[0481] drive TFT11a The configuration of drawing 69 is the approach of solving the technical problem by existence of parasitic capacitance 404 that writing is insufficient, when it receives and drive capacity forms twice (N-1) as many TFT11an as this.

[0482] The difference between drawing 69 and drawing 1 (a) is the point of having added TFT11an-1 and TFT11f for switching of a drive other than drive TFT11a N-1 time. It explains focusing on the difference between drawing 1 and drawing 69. If a current with TFT11an-1 and TFT11a is added, having been referred to as TFT11an-1 constitutes so that it may increase N times. Simply, the channel width W2 of TFT11an-1 is increased N-1 time of the channel width W1 of TFT11a. For example, if it is N= 10, the channel width W2 of 1, then TFT11an-1 is 9 times the channel width W1 of TFT11a of this. Therefore, theoretically, if TFT11a passes the current of 1, TFT11an-1 has the capacity to pass a 9 times as many current as this.

[0483] In addition, when passing a N times as many current as this to the source signal line 18, in drawing 69, the drive current of TFT11an-1 was set to N-1 with the configuration of drawing 69 because a 1 time as many current as TFT11a which passes a current was added to EL element 15. With the configuration of drawing 71, since the current of TFT11b which passes a current to EL element 15 does not flow to the source signal line 18, TFT11n needs to increase a drive current N times.

[0484] In order to give explanation easy here, TFT11a shall presuppose that the current which becomes I1 is passed, and TFT11an-1 shall pass the current of In-1. Moreover, I1 + It is referred to as In-1=Iw (in this case, Iw carries out by N times the current I1 passed to EL element 15).

[0485] The electrical potential difference of Vgl will be impressed to a current program period for gate signal line 17a, and TFT 11b, 11f, and 11c will be in an ON state. Moreover, as for gate signal line 17b, the electrical potential difference of Vgh is impressed, and

TFT11d is an OFF state. Therefore, the electrical potential difference equivalent to the program current Iw is programmed by the capacitor 19. that is, I1+ In-1 =Iw (in this case, Iw makes it twice [N] the current I1 passed to EL element 15) -- a current flows to the source signal line 18.

[0486] Next, the electrical potential difference of Vgh will be impressed to EL element 15 for gate signal line 17a in the period which passes a current, and TFT 11b, 11f, and 11c will be in an OFF state. Therefore, the source signal line 18 and a pixel 16 are separated. Moreover, as for gate signal line 17b, the electrical potential difference of Vgl will be impressed, and TFT11d will be in an ON state. Therefore, the current I1 corresponding to the program Iw currents1/N flows to EL element 15.

[0487] By driving as mentioned above, a N times as many current as the current (current passed to an EL element) of a request value can be passed to the source signal line 18. Therefore, the effect of parasitic capacitance (stray capacity) 404 is excepted, and a current program can fully be performed to a capacitor 19. On the other hand, a current can be impressed to a request value at EL element 15.

[0488] In drawing 69, although TFT11an-1 with the current capacity of N-1 and one piece are produced to a pixel, it does not limit to this. As shown in drawing 70, two or more TFT(s) (drawing 70 TFT11n1 - TFT11n6) may be produced. Since actuation is the same as that of drawing 69, explanation is omitted.

[0489] drive TFT11a The configuration of drawing 69 is the approach of solving the technical problem by existence of parasitic capacitance 404 that writing is insufficient, when it receives and drive capacity forms twice (N-1) as many TFT11an as this.

[0490] The configuration of drawing 69 can be developed also in the current mirror method illustrated to drawing 21, drawing 43, and drawing 71. What is necessary is just to form TFT11n which has the drive capacity to be N times many as this so that it may illustrate to drawing 71. However, it changes with a current mirror configuration and TFT11f [like] does not have the need.

[0491] In drawing 71, the ratio of the channel width W2 of TFT11n and the channel width W1 of TFT11b is set to N:1. In order to give explanation easy here, TFT11b shall presuppose that the current which becomes I1 is passed, and TFT11n shall pass the current of In. Moreover, In = it is referred to as Iw (in this case, Iw carries out by N times the current I1 passed to EL element 15).

[0492] The electrical potential difference of Vgl will be impressed to a current program period for gate signal line 17a, and TFT(s) 11c and 11d will be in an ON state. Therefore, the electrical potential difference equivalent to the program current Iw is programmed by the capacitor 19. that is, In =Iw (in this case, Iw makes it twice [N] the current I1 passed to EL element 15) -- a current flows to the source signal line 18. In addition, as for a little TFT11c and TFT11d, it is desirable to be able to shift timing and to control an on-off condition. In this case, it is necessary to make separate the gate signal line which controls TFT11c, and the gate signal line which controls TFT11d, and to carry out an independent control.

[0493] Next, the electrical potential difference of Vgh will be impressed to EL element 15 for gate signal line 17a in the period which passes a current, and TFT(s) 11c and 11d will be in an OFF state. Therefore, the source signal line 18 and a pixel 16 are separated. Therefore, the current I1 corresponding to the program Iw currents1/N flows to EL element 15.

[0494] By driving as mentioned above, a N times as many current as the current (current passed to an EL element) of a request value can be passed to the source signal line 18. Therefore, the effect of parasitic capacitance (stray capacity) 404 is excepted, and a current program can fully be performed to a capacitor 19. On the other hand, a current can be impressed to a request value at EL element 15.

[0495] In addition, gate signal line 17b and TFT11e are prepared in order to control so that

only non-image display or 1-/N periods, such as drawing 30, pass a current to EL element 15 as drawing 40 explained. Therefore, in the configuration of drawing 71, when a 1-/N period carries out the pulse drive of the current which passes a further N times as many current as this to a sink and EL element 15, the problem by parasitic capacitance 404 that writing is insufficient is completely lost. Moreover, a black insertion display can be realized easily and a good movie display can be realized.

[0496] The configuration of drawing 71 is very effective. For example, with the configuration of only drawing 1, if it is going to realize N= 10, it is necessary to impress the current of the shape of 10 times as high a pulse as a request value to EL element 15. In this case, since the terminal voltage of EL element 15 becomes high, the need of designing a Vdd electrical potential difference highly comes out. Moreover, EL element 15 may deteriorate.

[0497] However, with the configuration of drawing 71, if channel width W2 of TFT11n is made into 5 times of TFT11b and it programs with a current high twice, it will be set to 5x2=10. Therefore, it is realizable if only one half of periods impress a twice as many current as this to EL element 15. Therefore, the problem on which EL element 15 deteriorates does not have to be lost, either, and it is not necessary almost to make a Vdd electrical potential difference high.

[0498] Conversely, if it is going to realize N= 10 only by TFT11n, it is necessary to make channel width W2 of TFT11n into 10 times of TFT11b with the configuration of drawing 71. If it increases 10 times, the formation area of TFT11n occupies most area of a pixel. Therefore, a pixel numerical aperture becomes very small, or it becomes unrealizable. However, with the configuration of drawing 71, since what is necessary is just to make channel width W2 of TFT11n into 5 times of TFT11b, sufficient pixel numerical aperture is realizable.

[0499] There are many implementation approaches of N= 10. It is an approach to make channel width W2 of TFT11n into twice TFT11b, make channel width W2 of an approach to carry out period impression of one fifth for a 5 times higher current at EL element 15, and TFT11n into 4 times of TFT11b, and carry out period impression of 1/2.5 for a 2.5 times higher current at EL element 15 etc. That is, it is because what is necessary is just to make it multiplication set to 10 in consideration of the design (channel width W2) of TFT11n, the current passed to an EL element, and its period. Therefore, the value of N can be designed freely.

[0500] In drawing 71, although TFT11n with the current capacity of N and one piece are produced to a pixel, it does not limit to this. As shown in drawing 72, two or more TFT(s) (drawing 72 TFT11n1 - TFT11n5) may be produced. Since actuation is the same as that of drawing 71, explanation is omitted.

[0501] The same of it being is [many implementation approaches of N= 10] said of the configuration of drawing 69. It is an approach to make channel width W2 of TFT11an-1 into 4 times of TFT11a, make an approach to carry out period impression of one half for a current high twice at EL element 15, and channel width W2 of TFT11an-1 into twice TFT11ab, and carry out period impression of one fifth for a 5 times higher current at EL element 15 etc. That is, it is because what is necessary is just to make it multiplication set to 10 in consideration of the design (channel width W2) of TFT11an-1, the current passed to an EL element, and its period. Therefore, the value of N can be designed freely.

[0502] The matter applicable also in drawing 69, drawing 70, drawing 75, drawing 82, and drawing 83 explained above is clear. That is, this invention forms the drive TFT with large channel width in each pixel, and increases the current which drives the source signal line 18. And while increasing the current passed to EL element 15 explained by drawing 31 etc., it is the approach or configuration which makes a predetermined period the current passed to EL element 15.

[0503] Moreover, the display explained by drawing 30, drawing 31, etc. is realizable by controlling turning on and off of TFT11d or TFT11e. By this display, animation display can be improved and brightness can be adjusted. Therefore, although [this invention] the current which is proportional to an EL element at N times or N is impressed to EL element 15, it does not limit to this. The configuration of passing the current not more than 1 predetermined time or predetermined it to EL element 15 may be used. Even in this case, it is because the effectiveness that animation display can be improved and brightness can be adjusted easily can be demonstrated.

[0504] Although the same is said of drawing 1 and drawing 69, in case TFT11d is made into an ON state, the property variation by the kink phenomenon of TFT11a can be controlled by making resistance high. This explained with the configuration of drawing 1 (b). The variation in the current which flows to TFT11a decreases by arranging TFT11e of drawing 1 (b) and impressing a Vbb electrical potential difference (Vgl < Vbb < Vgh) to the gate terminal of TFT11e.

[0505] Therefore, also in the pixel configuration of drawing 1 and drawing 69, it is desirable to impress a Vbb electrical potential difference to gate signal line 17b, and to make TFT11d turn on. That is, Vgh is impressed in an OFF state and TFT11d impresses Vbb in an ON state.

[0506] This control is easy. It is because what is necessary is just to carry out circuitry like drawing 74. The inverter of the output stage of shift register 22b is because Vgh and Vbb are impressed to Vgh by gate signal line 17b by the power source, then the OFF state and Vbb can impress them to gate signal line 17b by the ON state.

[0507] In addition, the on-off control of the gate signal line 17 presupposed that it is based on the data which a shift register 22 holds. However, the method which does not limit to control by the shift register 22, and does not form a shift register 22, but controls each gate signal line 17 uniquely may be used for the on-off control of the gate signal line 17. For example, the gate signal line 17 of the arbitration which outputs ON state voltage may be chosen in a multiplexer circuit. Moreover, it may be parallel and all gate signal lines may be pulled out, and you may constitute so that ON state voltage or OFF state voltage can be freely impressed to each gate signal line. Thus, it is not based on the maintenance data of a shift register 22, but turning on and off of the display screens 21, such as drawing 31, drawing 32, drawing 87, drawing 88, drawing 198, drawing 201, drawing 215, drawing 218, drawing 220, and drawing 221, or strength processing of luminance distribution becomes easy from that of constituting so that the gate signal line 17 of arbitration can be chosen.

[0508] In addition, like drawing 1 (b), it cannot be overemphasized that TFT11e which impresses a Vbb electrical potential difference may be formed or arranged separately so that it may illustrate to drawing 75. The same of this matter is said of a current mirror configuration. For example, TFT11f which impresses a Vbb electrical potential difference so that it may illustrate to drawing 76 may be formed or arranged separately. The same is said of the pixel configuration of drawing 54. TFT11f which impresses a Vbb electrical potential difference so that it may illustrate to drawing 77 may be formed or arranged separately.

[0509] In addition, in drawing 78, by separating into TFT 11a1 and the plurality of TFT11a2, and connecting a gate terminal to a cascade, drive TFT11a can control a kink phenomenon, and can also control property dispersion. This is the same also about TFT11b of TFT11a of drawing 1, drawing 21, drawing 43, and drawing 71, TFT11a of drawing 69, and TFT11b of drawing 71 (adopting as a configuration of TFT for a drive is desirable).

[0510] Drawing 70 It called and it was presupposed that TFT11n etc. is divided into plurality in drawing 72. What is necessary is just to control whether TFT11n1 divided as other configurations so that it might illustrate to drawing 73, and TFT11n2 are operated as an object for the improvement in a drive current by potential (Vgh or Vhl) impressed to gate signal line 17c. If TFT11f2 is made into an OFF state, the current which flows to the source

signal line 18 will be set to one half when TFT11n1 and TFT11n2 are operating. These control is good to determine from the image display data of a display panel, and a viewpoint of power consumption.

[0511] The difference between drawing 75 and drawing 82 is the point of having connected the gate terminal of switching TFT11f to gate signal line 17c. That is, the on-off condition of TFT11f is not influenced by the potential condition of gate signal line 17a, but it is in the point that original control is realizable.

[0512] TFT11n is in the condition that TFT11f was continuously separated from the pixel by the OFF state. Therefore, it becomes the pixel configuration of drawing 1 (a). If gate signal line 17c and gate signal line 17a are used short-circuiting in logic, it will become the configuration of drawing 75.

[0513] The trouble of drawing 75 is a point that dispersion appears in the current which flows to EL element 15 for every pixel, when the property gap of TFT11n, Vt of TFT11a, etc. has occurred for every pixel. If dispersion occurs on a current, a feeling of a rough deposit will come also out of the homogeneity display of a white raster etc. to a display image. In that respect, this problem is not generated with the configuration of drawing 1.

[0514] Therefore, the screen size of a display panel is small, and when there is little effect of parasitic capacitance 404, TFT11f is continuously used by the OFF state. The screen size of a display panel is large, and when effect of parasitic capacitance 404 cannot be solved only in actuation of TFT11a, gate signal line 17c is short-circuited with the logic of gate signal line 17a, and it drives by realizing the pixel configuration of drawing 75.

[0515] The circuit block which drives the pixel configuration of drawing 82 to drawing 84 is shown. Shift register 22c which drives gate signal line 17c is formed, and gate signal line 17c is driven. When driving with the pixel configuration of drawing 1, the data of ST3 are continuously set to L, and to gate signal line 17c, it controls continuously so that the electrical potential difference of Vgh is outputted. What is necessary is just to make the same the data input conditions (timing, logic, etc.) of shift registers 22c and 22a, when using it with the configuration of drawing 82.

[0516] The configuration of drawing 82 can also realize the configuration of a current mirror. The pixel configuration is shown in drawing 83. What is necessary is just to control whether divided TFT 11a1 and TFT11n are operated as an object for the improvement in a drive current by potential (Vgh or Vhl) impressed to gate signal line 17c to illustrate to drawing 83. If TFT11f is made into an OFF state, as for the current which flows to the source signal line 18, only TFT11a will operate.

[0517] Drawing 82 is the point of having connected the gate terminal of switching TFT11f to gate signal line 17c. That is, the on-off condition of TFT11f is not influenced by the potential condition of gate signal line 17a, but it is in the point that original control is realizable.

[0518] TFT11n is in the condition that TFT11f was continuously separated from the pixel by the OFF state. If gate signal line 17c and gate signal line 17a are used short-circuiting in logic, it will become the configuration of drawing 75.

[0519] Therefore, like the pixel configuration of drawing 82, the screen size of a display panel is small, and when there is little effect of parasitic capacitance 404, TFT11f is continuously used by the OFF state. The screen size of a display panel is large, and when effect of parasitic capacitance 404 cannot be solved only in actuation of TFT11a, gate signal line 17c is short-circuited with the logic of gate signal line 17a, a drive current is increased, and it drives. Also in the pixel configuration of drawing 83, the circuit block of drawing 84 is applicable.

[0520] In addition, shift register 22c which controls gate signal line 17c by the configuration of drawing 84 was formed newly, and was operated. However, it does not limit to this configuration. The control logic of gate signal line 17c is easy. It is because Vgl or a Vgh

electrical potential difference is only impressed to the gate terminal of switching TFT11f. What is necessary is just to impress a Vhg electrical potential difference to the gate terminal of all TFT11f in a viewing area 21, when not operating TFT11n. What is necessary is just to impress the potential of gate signal line 17a to gate signal line 17c, when operating TFT11n. Therefore, it is not necessary to use shift register 22c separately like drawing 84. That is, it is because what is necessary is just to add a gate circuit so that the data of shift register 22a may be outputted to gate signal line 17c as it is or the potential of all gate signal line 17c may serve as Vgh.

[0521] The drive approach of this invention is explained to below. By N Doubling the current passed to the source signal line 18, the effect of parasitic capacitance 404 is lost and good image display with resolution can be realized.

[0522] Drawing 87 is the explanatory view of other examples which increase the current which flows to a source signal line. It is the method which chooses two or more pixel lines as coincidence fundamentally, carries out the charge and discharge of the parasitic capacitance of a source signal line etc. with the current with which two or more pixel lines were united, and improves current write-in lack sharply. However, since two or more pixel lines are chosen as coincidence, the current which per pixel drives can be decreased. Therefore, the current which flows to EL element 15 can be decreased. Here, in order to give explanation easy, it explains as N= 10 as an example (the current passed to a source signal line is increased 10 times).

[0523] In this invention explained by drawing 87 etc., a pixel line chooses a K pixel line as coincidence. From the source driver IC, N double current of a predetermined current is impressed to the source signal line 18. A N/K twice as many current as the current passed to an EL element is programmed by each pixel. In order to make an EL element into predetermined luminescence brightness, time amount which flows to an EL element is made into the K/N time amount of one frame. Thus, by driving, the charge and discharge of the parasitic capacitance of the source signal line 18 can fully be carried out, and predetermined luminescence brightness can be obtained for good resolution.

[0524] That is, as for a sink and other periods (1F (N-1) K/N), during the period of K/N of one frame does not pass a current for a current to an EL element. In this display condition, image data display and a black display (astigmatism LGT) are repeatedly displayed on every 1F. That is, an image data display condition will be in a discontinuous display (intermittent display) condition in time. Therefore, profile dotage of an image is lost and a good movie display can be realized. Moreover, since it drives with a N times as many current as this to the source signal line 18, effect of parasitic capacitance is not received but it can respond also to a highly minute display panel.

[0525] First, in order to make an understanding easy, the 1-pixel line explained above is chosen, and the method which programs a N times as many current as this is explained, referring to a drive wave etc. Drawing 134 is the explanatory view. In addition, although the screen is illustrated oblong with the explanatory view, it may not limit to this, and it may be longwise, and other configurations, such as a round shape, are sufficient.

[0526] Drawing 134 (a) is illustrating the write-in condition to a display image 21. In drawing 134 (a), 871 is a write-in pixel line. In addition, in drawing 134 (a), there is one pixel line written in 1H period. Moreover, although the pixel configuration of drawing 1 is mentioned as an example in the following examples and being explained, it may not be limiting to this, either, but you may be the pixel configuration of current mirrors, such as drawing 21, drawing 43, and drawing 71. Moreover, it cannot be overemphasized that it is applicable also to the pixel configuration of electrical-potential-difference program methods, such as drawing 54, drawing 67, drawing 68, and drawing 103.

[0527] In drawing 134 (a), if gate signal line 17a is chosen, the current which flows to the

source signal line 18 will be programmed by TFT11a. At this time, OFF state voltage is impressed and, as for gate signal line 17b, a current does not flow to EL element 15. It is because this has the capacity component of EL element 15 visible to an EL element side from the source signal line 18 in TFT11d being an ON state, it is influenced by this capacity and a current program exact enough becomes impossible to a capacitor 19. Therefore, the pixel line in which the current is written as shown in drawing 134 (b) will be in the astigmatism LGT condition 312. TFT11d of other pixel lines is an ON state, and is in the lighting condition 311. In addition, with the pixel configuration of the current mirror shown in drawing 21, drawing 43, drawing 71, etc., even if it is in the condition that a current flows to TFT11a which performs a current program, from the source signal line 18, EL element 15 is not visible. Therefore, as shown in drawing 134 (b), it is not necessary to consider as an astigmatism LGT condition. That is, it is not the indispensable condition of invention to write in, as shown in drawing 134 (b), and to use a pixel line as astigmatism LGT 312.

[0528] Drawing 135 is a voltage waveform impressed to the gate signal line 17. A voltage waveform sets OFF state voltage to Vgh (H level), and is setting ON state voltage to Vgl (L level). The number of the pixel line chosen as the lower berth of drawing 135 is indicated. Moreover, (1) and (2) show the chosen pixel line number.

[0529] In drawing 135, gate signal line 17a (1) is chosen (Vgl electrical potential difference), and a program current flows from TFT11a of the selected pixel line to the source signal line 18 toward the source driver 14. This program current is N times (in order to give explanation easy, it explains as N= 10.) of a predetermined value. of course, since a predetermined value is a data current which displays an image, unless it is white raster display etc., it is not a fixed value. it is . Therefore, it is programmed by the capacitor 19 so that a current flows 10 times at TFT11a. When the pixel line (1) is chosen, with the pixel configuration of drawing 1, OFF state voltage (Vgh) is impressed and, as for gate signal line 17b (1), a current does not flow to EL element 15.

[0530] After 1H, gate signal line 17a (2) is chosen (Vgl electrical potential difference), and a program current flows from TFT11a of the selected pixel line to the source signal line 18 toward the source driver 14. This program current is N times (in order to give explanation easy, it explains as N= 10) the predetermined value. Therefore, it is programmed by the capacitor 19 so that a current flows 10 times at TFT11a. When the pixel line (2) is chosen, with the pixel configuration of drawing 1, OFF state voltage (Vgh) is impressed and, as for gate signal line 17b (2), a current does not flow to EL element 15. However, since OFF state voltage (Vgh) is impressed to gate signal line 17of previous pixel line (1) a (1) and ON state voltage (Vgl) is impressed to gate signal line 17b (1), it is in the lighting condition.

[0531] After the following 1H, gate signal line 17a (3) is chosen, OFF state voltage (Vgh) is impressed and, as for gate signal line 17b (3), a current does not flow to EL element 15 of a pixel line (3). However, since OFF state voltage (Vgh) is impressed to gate signal line 17of previous pixel line (1) and (2) a (1), and (2) and ON state voltage (Vgl) is impressed to gate signal line 17b (1) and (2), it is in the lighting condition.

[0532] Synchronizing with the synchronizing signal of 1H, the image is displayed for the above actuation. However, by the drive method of drawing 135, a 10 times as many current as this flows to EL element 15. Therefore, the display screen 21 is displayed by one about 10 times the brightness of this. Of course, in order to perform a brightness display predetermined in this condition, it cannot be overemphasized that what is necessary is just to make a program current into 1/10. However, since it will write in with parasitic capacitance etc. and lack will occur if it is 1/10 of currents, it programs with a high current and the fundamental main point of this invention obtains predetermined brightness by black screen 312 insertion.

[0533] However, the approaches of drawing 134 are also the criteria of this invention. That is, it is the concept that make it a current higher than a predetermined current flow to EL

element 15, and it fully carries out the charge and discharge of the parasitic capacitance of the source signal line 18. That is, it is not necessary to pass a N times as many current as this to EL element 15. For example, a current path is formed in juxtaposition at EL element 15, it may shunt that a dummy EL element is formed, this EL element forms a light-shielding film, and light is not made (emit) toward a dummy EL element and EL element 15, and they may pass a current. [it] For example, when the signal current is 0.2microA, 2.2microA is passed to TFT11a, using a program current as 2.2microA. 0.2micro of signal currents A is passed to EL element 15 among this current, and 2microA is passed to a dummy EL element.

[0534] by constituting as mentioned above, a twice [N] as many current as this flows to drive TFT11a by making the current passed to the source signal line 18 increase N twice -- as -- the current sufficiently smaller programmable than N twice to current EL element 15 -- ****** -- things will be made. by the above approach, without forming the astigmatism LGT field 312 so that it may illustrate to drawing 136 etc., as shown in drawing 134, it is mostly -- it is -- all the viewing areas 21 can be completely made into the image display field 311.

[0535] However, if workmanship of forming a dummy EL element etc. is not carried out, the programmed current flows to EL element 15 theoretically [all]. Therefore, in drawing 134, the display screen emits light by one N times the brightness of this. What is necessary is just to form the astigmatism LGT viewing area 312 so that this may be illustrated in drawing 136 to make light emit by predetermined brightness. Drawing 136 is an explanatory view of the method.

[0536] Drawing 136 (a) is illustrating the write-in condition to a display image 21. In drawing 136 (a), 871a is a write-in pixel line. A program current is supplied to each source signal line 18 from a driver IC 14. In addition, in drawing 136, there is one pixel line written in 1H period. However, not a limiting [to 1H]-in any way thing but 0.5H period or 2H period is sufficient. Moreover, although a program current is written in the source signal line 18, this invention is not limited to a current program method, and the electrical-potential-difference program method which is an electrical potential difference may be written in the source signal line 18.

[0537] In drawing 136 (a), like drawing 134, if gate signal line 17a is chosen, the current which flows to the source signal line 18 will be programmed by TFT11a. At this time, OFF state voltage is impressed and, as for gate signal line 17b, a current does not flow to EL element 15. It is because this has the capacity component of EL element 15 visible to an EL element side from the source signal line 18 in TFT11d being an ON state, it is influenced by this capacity and a current program exact enough becomes impossible to a capacitor 19. Therefore, if the configuration of drawing 1 is made into an example, the pixel line in which the current is written as shown in drawing 136 (b) will serve as the astigmatism LGT field 312.

[0538] If now programmed with the twice [N (here, as stated previously, referred to as N= 10)] as many current as this, the brightness of a screen increases 10 times. Therefore, what is necessary is just to let 90% of range of a viewing area 21 be the astigmatism LGT field 312. Therefore, the horizontal scanning line of an image display field considers as 220 (S= 220) then 22, and the viewing area 311 of QCIF, and should just 220-22=198 make it the non-display field 312. If it generally states, S, then the field of S/N will be made into a viewing area 311 for a horizontal scanning line (pixel line count), and this viewing area 311 will be made to emit light by one N times the brightness of this. And this viewing area 311 is scanned in the vertical direction of a screen. Therefore, let the field of S (N-1)/N be the astigmatism LGT field 312. This astigmatism LGT field is a black display (nonluminescent). Moreover, this nonluminescent section 312 is realized by making TFT11d turn off. In addition, although carried out to making the light switch on by one N times the brightness of this, it cannot be overemphasized that it adjusts with one N times the value of this by

brightness adjustment and gamma adjustment with a natural thing.

[0539] Moreover, in the previous example, if programmed with the 10 times as many current as this, the brightness of a screen increased 10 times and it was presupposed that what is necessary is just to make 90% of range of a viewing area 21 into the astigmatism LGT field 312. However, this does not limit the pixel of RGB to considering as the astigmatism LGT field 312 in common. For example, the pixel of R may make one eighth the astigmatism LGT field 312, the pixel of G may make one sixth the astigmatism LGT field 312, and the pixel of B may change 1/10 in the astigmatism LGT field 312 and each color. Moreover, you may enable it to adjust the astigmatism LGT field 312 (or lighting field 311) according to an individual by the color of RGB. In order to realize these, gate signal line 17b of an individual exception is needed by R, G, and B. However, by enabling individual adjustment of the above RGB, it becomes possible to adjust a white balance and balance adjustment of a color becomes easy in each gradation.

[0540] The pixel line containing write-in pixel line 871a considers as the astigmatism LGT field 312, and makes the range of S/N of an upper screen a viewing area 311 so that it may illustrate rather than write-in pixel line 871a to drawing 136 (b) (when a write-in scan scans a screen from the bottom upwards to in a down case, it serves as the reverse from on a screen). A viewing area 311 becomes band-like and moves an image display condition downward from on a screen.

[0541] Drawing 137 is a voltage waveform impressed to the gate signal line 17. A voltage waveform sets OFF state voltage to Vgh (H level), and is setting ON state voltage to Vgl (L level). The number of the pixel line chosen as the lower berth of drawing 137 is indicated. Moreover, (1), (2), (3) -- The pixel line number chosen with - is shown.

[0542] In drawing 137, gate signal line 17a (1) is chosen (Vgl electrical potential difference), and a program current flows from TFT11a of the selected pixel line to the source signal line 18 toward the source driver 14. This program current is N times (in order to give explanation easy, it explains as N= 10.) of a predetermined value. of course, since a predetermined value is a data current which displays an image, unless it is white raster display etc., it is not a fixed value. it is .

[0543] Therefore, it is programmed by the capacitor 19 so that a current flows 10 times at TFT11a. When the pixel line (1) is chosen, with the pixel configuration of drawing 1, OFF state voltage (Vgh) is impressed and, as for gate signal line 17b (1), a current does not flow to EL element 15.

[0544] 1H (of course, it does not limit to 1H.) It is for giving explanation easy. Behind, gate signal line 17a (2) is chosen (Vgl electrical potential difference), and a program current flows from TFT11a of the selected pixel line to the source signal line 18 toward the source driver 14. This program current is N times (in order to give explanation easy, it explains as N= 10) the predetermined value. Therefore, it is programmed by the capacitor 19 so that a current flows 10 times at TFT11a. At this time, as for gate signal line 17b (1), a Vgl electrical potential difference (ON state voltage) is impressed. According to the example of drawing 136, the period when this ON state voltage is impressed is a period of S/N. Then, Vgh (OFF state voltage) is impressed and, as for gate signal line 17b (1), a current does not flow to EL element 15 of a pixel line (1).

[0545] When the pixel line (2) is chosen, with the pixel configuration of drawing 1, OFF state voltage (Vgh) is impressed and, as for gate signal line 17b (2), a current does not flow to EL element 15. However, since OFF state voltage (Vgh) is impressed to gate signal line 17of previous pixel line (1) a (1) and ON state voltage (Vgl) is impressed to gate signal line 17b (1), it is in the lighting condition. According to the example of drawing 136, the period when this ON state voltage is impressed is a period of S/N. Then, Vgh (OFF state voltage) is impressed and, as for gate signal line 17b (2), a current does not flow to EL element 15 of a

pixel line (2).

[0546] After the following 1H, gate signal line 17a (3) is chosen, OFF state voltage (Vgh) is impressed and, as for gate signal line 17b (3), a current does not flow to EL element 15 of a pixel line (3). However, since OFF state voltage (Vgh) is impressed to gate signal line 17of previous pixel line (1) and (2) a (1), and (2) and ON state voltage (Vgl) is impressed to gate signal line 17b (1) and (2), it is in the lighting condition. The above actuation is repeated and the display condition of drawing 136 is realized.

[0547] In the display of drawing 136, one viewing area 311 moves to down from on a screen. If a frame rate is low, it will be recognized visually that a viewing area 311 moves. It becomes that it is easy to be recognized when a palpebra is closed especially, or when moving a face up and down.

[0548] It is good to divide a viewing area 311 into plurality so that it may illustrate to drawing 138 to this technical problem. Drawing 138 (b) is dividing the non-display field 312 into five. If the part which added these five serves as area of S (N-1)/N, it will become the brightness and the EQC of drawing 136. Conversely, if it sees from a viewing area 311, the viewing area (lighting field) 311 will be divided into six, but if it constitutes so that the part which added the field divided into these six may carry out abbreviation coincidence with S/N (drive), it will become equivalent to the display brightness of drawing 136.

[0549] In addition, it is not necessary to make equal the divided viewing area 311 so that it may illustrate to drawing 138 (b). Moreover, it is not necessary to also make equal the divided non-display field 312.

[0550] As mentioned above, a flicker of a screen decreases by dividing a viewing area 311 into plurality. Therefore, there is no generating of a flicker and it can realize good image display. In addition, division may be made finer. However, the more it divides, the more the animation display engine performance falls.

[0551] Drawing 139 is a voltage waveform impressed to the gate signal line 17. The difference between drawing 139 and drawing 137 is actuation of gate signal line 17b. Gate signal line 17b carries out on-off (Vgl and Vgh) actuation by the number corresponding to the number which divides a screen. Since other points are the same as that of drawing 137, explanation is omitted.

[0552] In the above example, the pixel line chosen as coincidence was a 1-pixel line. Drawing 88 is the approach of choosing two or more pixel line as coincidence. Although it explains by drawing 88 choosing it as a 5-pixel line and coincidence in order to give explanation easy, not to be limiting to this, either but what is necessary is just 2 pixels or more. However, an increment of the pixel line chosen as coincidence reduces the variation absorption effect of drive TFT11a.

[0553] In addition, although explained by illustrating the pixel configuration of the current program of drawing 1 also in the following examples, it does not limit to this. It cannot be overemphasized that it is effective also by drawing 21, drawing 43, and the current mirror of drawing 71. By [which the pixel line chosen as coincidence sets] becoming, it is because charges and discharges, such as the parasitic capacitance 404 of a source signal line, become easy. Moreover, the pixel configuration of electrical-potential-difference programs, such as drawing 54, drawing 67, drawing 68, and drawing 103, is also effective. When the pixel line chosen as coincidence increases, it is because the preliminary charge of the adjoining pixel line can be carried out and it can respond also to a highly minute display panel.

[0554] In addition, in order to give explanation easy, the current (or the current which the source driver IC 14 absorbs from the source signal line 18, the current which drive TFT11a slushes into the source signal line 18) passed from the source driver IC 14 to the source signal line 18 explains as 10 times (N= 10) of a predetermined value also here.

[0555] Therefore, if the pixel line chosen as coincidence is a 5-pixel line (K= 5), five drive

TFT11a will operate. That is, per pixel, and 10 / 5= 2 twice as many current as this flows to TFT11a. If the pixel line chosen as coincidence is a 2-pixel line, two drive TFT11a will operate. That is, per pixel, and 10 / 2= 5 times as many current as this flows to TFT11a.

[0556] If the pixel line chosen as coincidence is a 5-pixel line (K= 5), it will become what added five program currents of TFT11a. For example, originally, it considers as the current Id to write in and the current of Idx10 is passed to N= 10, then the source signal line 18 at write-in pixel line 871a. Pixel line 871b which adjoined write-in pixel line 871a (871b is a pixel line used auxiliary in order to make the amount of currents to the source signal line 18 increase.) Therefore, the pixel (line) which writes in an image is 871a, and in order to write in 871a, 871b uses [a pixel (line)] auxiliary.

[0557] Ideally, 5-pixel TFT11a passes the current of Idx2 to the source signal line 18, respectively. And a twice as many current as this is programmed by the capacitor 19 of each pixel 16. However, actually, since the property has shifted, variation generates each 5-pixel TFT11 on the current programmed by the capacitor 19 of each pixel. For example, a 2.2 times, 2.0 times, 1.6 times, and 2.4 times as many current as this is programmed by 1.8 time and four pixel (line) 871b at pixel (line) 871a. In this example, a 1.8 times as many current as this is programmed by write-in pixel line 871a. Therefore, (2.0-1.8) / 2.0= 10% of error comes out. However, the current adding these is maintained at 10 times and default value.

[0558] That is, to the source signal line 18, the current programmed from the source driver 14 flows as a convention. However, the current to which property variation responded to the selected pixel flows. Therefore, a target program current shifts from the set point, so that the property variation of TFT11a of each pixel is large. However, since the property of adjoining TFT11a corresponds mostly, even if it makes the pixel line chosen as coincidence like drawing 88 increase, it can realize a homogeneity display.

[0559] In addition, examples, such as drawing 87 and drawing 88, are effective in the display panel which formed TFT11 with the low-temperature polish recon technique, and formed TFT11 with the amorphous silicon technique rather than the display panel. In TFT11 of an amorphous silicon, it is because the property of adjoining TFT is mostly in agreement. Therefore, even if it drives with the added current, the drive current of each TFT serves as desired value mostly.

[0560] In drawing 88, it writes in K line (K= 5) coincidence by the image data of write-in pixel (line) 871a. Therefore, the range of K lines (871a, 871b) serves as the same display. Thus, if it is made the same display, resolution will fall with a natural thing. In order to cope with this, it writes in so that it may illustrate to drawing 88 (b), and the part of the pixel line 871 is considered as the astigmatism LGT display 312. Therefore, a resolution fall is not generated.

[0561] After the following 1H writes in the location which carried out the 1-pixel line shift, and performs the same actuation as pixel line 871a. The 1-pixel (line) shift also of the astigmatism LGT field 312 is carried out. Therefore, the pixel (line) by which the current program was carried out by 1H of the point is displayed.

[0562] As mentioned above, 871b in which different current data from an original indicative data were written is not displayed. If it shifts the above actuation of one line at a time, perfect image display is realizable. Moreover, the charge and discharge of parasitic capacitance 404 are also realizable within 1H period enough by the effectiveness of pixel line 871b used auxiliary.

[0563] Drawing 140 is an explanatory view of a drive wave for realizing the drive approach of drawing 88. Like drawing 135, a voltage waveform sets OFF state voltage to Vgh (H level), and is setting ON state voltage to Vgl (L level). Moreover, the number of the pixel line chosen as the lower berth of drawing 140 is indicated. Moreover, (1), (2), (3) ... (6) shows the chosen pixel line number. Therefore, in the case of, in the case of a QCIF display panel, it is

220, and a line count is 480 by the VGA panel.

[0564] In drawing 140, gate signal line 17a (1) is chosen (Vgl electrical potential difference), and a program current flows from TFT11a of the selected pixel line to the source signal line 18 toward the source driver 14. Here, in order to give explanation easy, it explains first that write-in pixel line 871a is eye pixel line (1) watch.

[0565] Moreover, the program current which flows to the source signal line 18 is N times (in order to give explanation easy, it explains as N= 10.) of a predetermined value. of course, since a predetermined value is a data current which displays an image, unless it is white raster display etc., it is not a fixed value. it is . Moreover, a 5-pixel line explains to coincidence as selection (K= 5). Therefore, ideally, it is programmed by the capacitor 19 of one pixel so that a current flows twice at TFT11a.

[0566] When a write-in pixel line is eye (1) pixel line, as illustrated in drawing 140, as for gate signal line 17a, (1), (2), (3), (4), and (5) are chosen. That is, switching TFT11b of a pixel line (1), (2), (3), (4), and (5) and TFT11c are ON states. Moreover, gate signal line 17b is the opposite phase of gate signal line 17a. Therefore, the current is not flowing to EL element 15 of the pixel line which switching TFT11d of a pixel line (1), (2), (3), (4), and (5) is an OFF state, and corresponds. That is, it is in the astigmatism LGT condition 312.

[0567] Ideally, 5-pixel TFT11a passes the current of Idx2 to the source signal line 18, respectively. And a twice as many current as this is programmed by the capacitor 19 of each pixel 16. Here, in order to make an understanding easy, it explains noting that the property (Vt, S value) of each TFT11a corresponds.

[0568] Since the pixel line chosen as coincidence is a 5-pixel line (K= 5), five drive TFT11a operates. That is, per pixel, and 10 / 5= 2 twice as many current as this flows to TFT11a. In the source signal line 18, the current which added five program currents of TFT11a flows. For example, originally, it considers as the current Id to write in and the current of Idx10 is passed to the source signal line 18 at write-in pixel line 871a. In order to make the amount of currents to the write-in pixel line 871b source signal line 18 which writes in image data henceforth increase from a write-in pixel line (1), it is the pixel line used auxiliary. However, since the image data of normal is written in behind, write-in pixel line 871b is satisfactory.

[0569] Therefore, pixel line 871b is the same display as 871a between 1H periods. Therefore, pixel line 871b chosen in order to make write-in pixel line 871a and a current increase is made into the non-display condition 312 at least. However, with the pixel configuration of electrical-potential-difference program methods, such as drawing 21, drawing 43, a pixel configuration of a current mirror like drawing 71, and drawing 68, it is good also as a display condition depending on the case.

[0570] After the following 1H, gate signal line 17a (1) is un-choosing, and ON state voltage (Vgl) is impressed to gate signal line 17b. Moreover, gate signal line 17a (6) is chosen as coincidence (Vgl electrical potential difference), and a program current flows from TFT11a of the selected pixel line (6) to the source signal line 18 toward the source driver 14. Thus, from that of operating, the image data of normal is held at a pixel line (1).

[0571] After the following 1H, gate signal line 17a (2) is un-choosing, and ON state voltage (Vgl) is impressed to gate signal line 17b. Moreover, gate signal line 17a (7) is chosen as coincidence (Vgl electrical potential difference), and a program current flows from TFT11a of the selected pixel line (7) to the source signal line 18 toward the source driver 14. Thus, from that of operating, the image data of normal is held at a pixel line (2). one screen is rewritten by scanning, shifting a 1-pixel line every with the above actuation.

[0572] Although it is the same as that of drawing 134, in order to program with a twice as many current (electrical potential difference) as this to each pixel, by the drive approach of drawing 140, the luminescence brightness of EL element 15 of each pixel becomes twice ideally. Therefore, the brightness of the display screen becomes twice from a predetermined

value.

[0573] What is necessary is just to let one half of the range of a viewing area 21 be the non-display fields 312, including the write-in pixel line 871 so that you may illustrate to drawing 87 in order to make this into predetermined brightness. Since this was explained using drawing 137 etc., it omits explanation.

[0574] The animation display engine performance improves, so that area of the black viewing area (non-display field) 312 occupied to the display screen 21 is enlarged. Therefore, what is necessary is to lessen the non-display field 311 so that it may illustrate to drawing 141, and just to enlarge area of the non-display field 312.

[0575] Like drawing 87, by twice, the current programmed to each pixel can obtain predetermined display brightness, if the area of the lighting field 311 is 1/2 of the display screen 21. However, as shown in drawing 141, a screen becomes dark when the lighting field 311 is smaller than one half of the display screens 21. What is necessary is just to enlarge the current programmed to each pixel, in order to obtain predetermined brightness. For example, what is necessary is for a viewing area (lighting field) 311 to be 1/5 of the area of the display screen 21, and just to increase the current (electrical potential difference) programmed in a 1-pixel line 5 times of a predetermined value, if the number of the pixel lines chosen as coincidence is five (K= 5). The current which flows to the source signal line 18 becomes 5x5 pixel line =25 time.

[0576] Anyway, in the example of this invention, a program current (electrical potential difference) can be adjusted by changing the current (electrical potential difference) passed to the source signal line 18. That is, the current which flows to the source signal line 18 can be adjusted only by adjusting the reference current (electrical potential difference) of the source driver 14. It can be set up by the data to ST* terminal impressed to the shift register 22 of the gate driver 12 illustrated to drawing 2 etc. whether coincidence is made whether coincidence is made to turn on a 2-pixel line or to turn on a 5-pixel line or only a 1-pixel line is chosen. Therefore, the specification of the source driver 14 is not influenced by the number of pixels to choose. Moreover, since the brightness of a screen can also be adjusted by turning on and off of gate signal line 17b, the output current from the source driver 14 is not changed by brightness adjustment of Screen 21. Therefore, what is necessary is just to determine the gamma property of EL element 15 to one current. Therefore, the configuration of the source driver 14 is very easy, and becomes the high thing of versatility. It cannot be overemphasized that the above matter is applicable also to the example of other this inventions.

[0577] The above example was a configuration which arranges one selection pixel line for every 1-pixel line (formation). This invention may not be limited to this and may arrange one selector-gate signal line in two or more pixel lines (formation).

[0578] Drawing 294 is the example. In addition, in order to give explanation easy, a pixel configuration explains by mainly illustrating the case of drawing 1. In drawing 294, selector-gate signal-line 17a of a pixel line chooses three pixels (16R, 16G, 16B) as coincidence. The notation of R means red pixel relation, the notation of G shall mean green pixel relation and the notation of B shall mean blue pixel relation.

[0579] Therefore, pixel 16R, pixel 16G, and pixel 16B is chosen as coincidence by selection of gate signal line 17a, and will be in a data write-in condition by it. Pixel 16R writes data in capacitor 19R from source signal-line 18R, and pixel 16G write data in capacitor 19G from source signal-line 18G. Pixel 16B writes data in capacitor 19B from source signal-line 18B.

[0580] TFT11d of pixel 16R is connected to gate signal line 17bR. Moreover, TFT11d of pixel 16G is connected to gate signal line 17bG, and TFT11d of pixel 16B is connected to gate signal line 17bB. Therefore, on-off control of EL element15R of pixel 16R, EL element 15G of pixel 16G, and the EL element 15of pixel 16B B can be carried out separately. That is, EL element15R, EL element 15G, and EL element 15B are controllable according to an

individual in lighting time amount and a lighting period by controlling each gate signal line 17bR, 17bG, and 17bB.

[0581] In order to realize this actuation, in the configuration of drawing 2, it is appropriate to form four, the shift register 22 which scans gate signal line 17a, the shift register 22 which scans gate signal line 17bR, the shift register 22 which scans gate signal line 17bG, and the shift register 22 which scans gate signal line 17bB, (arrangement).

[0582] Drawing 295 is illustrating arrangement of a pixel 16. In drawing 295, the pixel is formed in the shape of horizontal SUTORAIBU (generally with the still more conventional configuration, it is a vertical stripe-like). By arranging a pixel in the shape of a horizontal stripe, connection between the gate signal line 17 and a switching element 11 becomes easy, and a pixel layout also becomes easy. Moreover, in the EL element of polymeric materials, production by the ink jet also becomes easy.

[0583] In addition, although [in drawing 294 and drawing 295] a pixel is formed in the shape of horizontal SUTORAIBU, it cannot be overemphasized that you may be a vertical stripe-like as usual. Moreover, it cannot be overemphasized that it is appropriate to combine with other examples explained on these specifications, such as a configuration which adds the configuration which explains henceforth or makes separate the electrical potential difference of the reverse bias electrical-potential-difference impression method which explained, a block drive method, the control system in a Vbb electrical potential difference, and each RGB, the method which TFT11b runs and uses an electrical potential difference, the method of drawing 241, and a dummy pixel line.

[0584] Drawing 296 is the wave of the pixel configuration of drawing 294 of operation. In addition, in order to give explanation easy, it explains noting that a 1-pixel line (it will be called a 3-pixel line, of course if it counts by RGB) is chosen. However, it cannot be overemphasized that the drive approach which chooses two or more pixel lines as coincidence as drawing 87, drawing 88, drawing 142, etc. explained is also realizable. Moreover, as drawing 252 explained, even if it is the range of 1H period, it is necessary to perform timing control of a gate signal line but, and in order to give explanation easy here, selection of the pixel line by gate signal line 17a explains noting that it is 1H period. The above matter is applied also in other drive approaches explained on these specifications, and a panel configuration.

[0585] In drawing 296, when a write-in pixel line is eye (1) pixel line, pixel 16 block (as for an understanding, the direction which considers this to be a 1-pixel line becomes easy) has chosen gate signal line 17a (also set and refer to drawing 294). That is, pixel 16R, pixel 16G, and pixel 16B are chosen. Therefore, switching TFT11b of 16G of 16R of a pixel line (1) and a pixel line (1) and 16B of a pixel line (1) and TFT11c are ON states.

[0586] Pixel 16R of a pixel line (1) writes the image data from source signal-line 18R in capacitor 19R. Moreover, pixel 16G of a pixel line (1) write the image data from source signal-line 18G in capacitor 19G, and pixel 16B of a pixel line (1) writes the image data from source signal-line 18B in capacitor 19B.

[0587] In addition, in order to give explanation easy, it supposes that it programs so that a N times (N= 2) as many current as this flows to each pixel at EL element 15, and drawing 296 explains noting that a current flows to EL element 15 at the period of 1-/N of one frame (1 field). However, it cannot be overemphasized that other examples may be carried out as this specification explains. Moreover, it cannot be overemphasized by enlarging N-ary that the effect of the parasitic capacitance 404 of the source signal line 18 can be disregarded now, and it becomes easy to write image data in a pixel 16. That is, it does not limit to N= 2. Moreover, it cannot be overemphasized that N is not limited to an integer and it can realize also with values, such as 2.5. Moreover, the selection time amount of gate signal line 17a may not be limited to 1H, either, and more than 2H is sufficient as it.

[0588] Gate signal line 17bR of a pixel line (1), gate signal line 17bG, and gate signal line 17bB serve as an opposite phase of gate signal line 17a. Therefore, the current is not flowing to the EL element (15R, 15G, 15B) of the pixel line which switching TFT11d of pixel 16R [of a pixel line (1)], pixel 16G, and pixel 16B is an OFF state at least, and corresponds. That is, it is in the astigmatism LGT condition 312.

[0589] After the following 1H, gate signal line 17a (1) is un-choosing, and ON state voltage (Vgl) is impressed to gate signal line 17b. Moreover, gate signal line 17a (2) is chosen as coincidence (Vgl electrical potential difference), and a program current flows toward the source driver 14 to the source signal line 18 (G respectively 18R, 18 18B) from TFT11a of pixel 16R [of the selected pixel line (2)], pixel 16G, and pixel 16B. Thus, by operating, image data is held at pixel 16R [of a pixel line (1)], pixel 16G, and pixel 16B.

[0590] Furthermore, after the following 1H, gate signal line 17a (2) is un-choosing, and ON state voltage (Vgl) is impressed to gate signal line 17b (2). Moreover, gate signal line 17a (3) is chosen as coincidence (Vgl electrical potential difference), and a program current flows from TFT11a of the selected pixel line (3) to the source signal line 18 toward the source driver 14. Thus, from that of operating, image data is held at a pixel line (2). one screen is rewritten by scanning shifting the above actuation a 1-pixel line every.

[0591] Next, actuation of gate signal line 17b of drawing 296 is mainly explained. Gate signal line 17bR is connected to pixel 16R. Gate signal line 17bG is connected to pixel 16G. Moreover, gate signal line 17bB is connected to pixel 16B. Therefore, pixel 16R can carry out on-off control of the current which flows to EL element 15R by gate signal line 17bR. Similarly, pixel 16G can carry out on-off control of the current which flows to EL element 15G by gate signal line 17bG, and pixel 16B can carry out on-off control of the current which flows to EL element 15B by gate signal line 17bB.

[0592] In drawing 296, gate signal line 17bR, gate signal line 17bG, and gate signal line 17bB are made into the same waveform in each pixel line. Therefore, EL elements 15R, 15G, and 15B are turned on and off by coincidence (lighting, astigmatism LGT). In addition, although drawing 296 is making every 4H turn on and turn off EL element 15, it is not limited to this. Every 1H and more than it are sufficient. Moreover, EL element 15 may be made to turn on and off with the period not more than 1H theoretically.

[0593] However, if an on-off period is made too much quick, animation dotage will occur in a movie display. Therefore, it is necessary to set spacing until it turns on, and EL element 15 puts out the light and then turns on to 0.5 or more msecs. When this period was short, it will not be in a perfect black display condition with the after-image property of human being's eyes, but an image came to have faded, and resolution came to have fallen. Moreover, it will be in the display condition of the display panel of a data-hold mold. However, when an on-off period is set to 100 or more msecs, it is visible to a flashing condition. Therefore, the on-off period of an EL element should be made 100 or less msec more than 0.5microsec. The on-off period should be made still more preferably 2 or more-msec 30 or less msec. The on-off period should be made still more preferably 3 or more-msec 20 or less msec.

[0594] The number of insertion of the black screen 312 made to turn a screen on and off is determined from the period or count of the time amount which one frame (1 field) takes from the above relation, and the signal (Vgh, Vgl) impressed to gate signal line 17b. Although a good movie display is realizable if the black screen 312 is set to one, a flicker of a screen becomes easy to be in sight. Therefore, it is desirable to divide the black 312 insertion section into plurality. However, if the number of partitions is made [many / too much], animation dotage will occur. The number of partitions should carry out to eight or less [1 or more]. It is desirable to carry out to five or less [1 or more] still more preferably.

[0595] In addition, this invention turns off TFT11d, and even if it intercepts the current which flows to EL element 15, if it turns on TFT11d, it can pass again the same current as the

current which was flowing previously to EL element 15. This is because memory (analog memory) of the current value to pass is carried out to the capacitor 19 of a pixel. This matter is the big description of this invention. That is, it is because control made to turn on and off the current passed to EL element 15 can be freed.

[0596] In drawing 296, gate signal line 17bR, gate signal line 17bG, and gate signal line 17bB are made into the same waveform in each pixel line. Moreover, selection of a pixel line is carrying out the cyst of the selection pixel line one by one to every 1H. Therefore, the luminescence location of EL elements 15R, 15G, and 15B is moved downward from on Screen 21 at the high speed. Moreover, the insertion rate of this on-off control and the black screen 312 and the insertion number of the black screen 312 are easily realizable by controlling ST data to the shift register 22 explained by drawing 2 etc. Of course, it cannot be overemphasized that parallel control of the control of the Vgh data impressed to gate signal line 17b may be carried out.

[0597] Moreover, although the signal impressed to the gate signal line 17 was made into the periodic signal, it may not be limited to this and an aperiodic signal is sufficient as it. However, if total of the time amount which turns on or turns off EL element 15 differs, the brightness of a screen will change. Moreover, a gap of color balance occurs. Therefore, it is necessary to set at the period of one frame (1 field), and to make into constant value total of the time amount which turns on or turns off EL element 15. When special, total of the time amount which turns on or turns off EL element 15 in the period more than two frame (2 field) is made [******] into constant value. They are the case where one frame (field) is very high-speed, and the case of an FSC (frame sequential control) drive.

[0598] In drawing 296, gate signal line 17bR, gate signal line 17bG, and gate signal line 17bB are made into the same waveform in each pixel line. Moreover, selection of a pixel line is carrying out the cyst of the selection pixel line one by one to every 1H. In drawing 297, the wave impressed to gate signal line 17bR is changed 2H period, the wave impressed to gate signal line 17bG is changed 3H period, and the wave impressed to gate signal line 17bB is changed 4H period. Since other matters are the same as that of drawing 296, explanation is omitted.

[0599] In addition, although [in drawing 297] the wave impressed to gate signal line 17bR is changed 2H period, the wave impressed to gate signal line 17bG is changed 3H period and the wave impressed to gate signal line 17bB is changed 4H period, this is for making a plot easy and is not limited to 2H, 3H, etc. The signal wave form impressed to one or more gate signal line 17b at least among gate signal line 16bR connected to pixel 16R, gate signal line 16bG connected to pixel 16G, and gate signal line 16bB connected to pixel 16B changes other gate signal line 17b.

[0600] If it drives as shown in drawing 297, the luminescence location of EL elements 15R, 15G, and 15B is moved downward from on Screen 21 at the high speed. Under the present circumstances, the on-off (lighting, astigmatism LGT) period of EL element 15R and the on-off (lighting, astigmatism LGT) period of EL element 15G differ from the on-off (lighting, astigmatism LGT) period of EL element 15B. By changing the lighting period of EL element 15, generating of a flicker stops being able to be conspicuous easily.

[0601] Moreover, the insertion rate of this on-off control and the black screen 312 and the insertion number of the black screen 312 are easily realizable by controlling ST data to the shift register 22 explained by drawing 2 etc. Of course, it cannot be overemphasized that parallel control of the control of the signal (Vgh, Vgl) data impressed to gate signal line 17b may be carried out.

[0602] In drawing 298, the Vgl period impressed to gate signal line 17bR is made shorter than other gate signal line 17b. Therefore, the lighting time amount of EL element 15R connected to gate signal line 17bR becomes long (the period which TFT11d of pixel 16R

turns on becomes long). Therefore, the luminescence brightness of R of the display screen 21 becomes strong.

[0603] As mentioned above, the color balance of Screen 21 and generating of a flicker can be controlled by controlling the signal impressed to gate signal line 17bR, gate signal line 17bG, and gate signal line 17bB according to an individual. That is, the color balance of Screen 21 and generating of a flicker can be controlled by controlling the time amount and timing which make EL element 15 turn on, and a period.

[0604] In addition, although [in drawing 298] the wave impressed to gate signal line 17bG is changed 3H period and the wave impressed to gate signal line 17bB is changed 4H period, this is for making a plot easy and is not limited to 2H, 3H, etc. The impression time amount of the signal which makes TFT11d turn on among the signal wave forms impressed to one or more gate signal line 17b at least among gate signal line 16bR connected to pixel 16R, gate signal line 16bG connected to pixel 16G, and gate signal line 16bB connected to pixel 16B (or it is made to turn off) changes other gate signal line 17b.

[0605] If it drives as shown in drawing 298, the luminescence location of EL elements 15R, 15G, and 15B is moved downward from on Screen 21 at the high speed. Under the present circumstances, the ON (lighting) time amount of EL element 15R, the ON (lighting) time amount of EL element 15G, and the ON (lighting) time amount of EL element 15B can be changed. Therefore, color balance adjustment of a screen is attained and generating of a flicker stops being able to be conspicuous easily. While a user sees Screen 21, as for such color balance adjustment, constituting so that it can adjust is desirable. This adjustment is easy. It is because what is necessary is just to increase or decrease the ON number of ST data inputted into the shift registers 22, such as drawing 2. Moreover, the insertion rate of this on-off control and the black screen 312 and the insertion number of the black screen 312 are easily realizable by controlling ST data to the shift register 22 explained by drawing 2 etc. Of course, it cannot be overemphasized that parallel control of the control of the signal (Vgh, Vgl) data impressed to gate signal line 17b may be carried out.

[0606] In addition, drawing 298 explained by illustrating the case where a pixel configuration is drawing 1 from drawing 294. However, it cannot be overemphasized that it is applicable even if the above examples are other pixel configurations. For example, they are drawing 21, drawing 43, drawing 71, drawing 22, drawing 54, drawing 68, drawing 103, etc. That is, the technical thought explained in drawing 298 is applicable also in other configurations from drawing 294. For example, drawing 360 is an example in the configuration (refer to drawing 21, drawing 43, etc.) of a pixel of a current mirror. Moreover, drawing 361 is the example of the pixel configuration of the electrical-potential-difference program illustrated by drawing 54 etc.

[0607] The drive approach explained in drawing 88, drawing 87, drawing 140, etc. was a drive method which chooses two or more pixel line as coincidence. Cautions are required of this drive method in respect of the following. If it says from a conclusion, it will be that what the pixel (line) (dummy pixel (line)) which does not contribute to a display is prepared for (it forms) is desirable. The above reason etc. is explained to below.

[0608] Drawing 246 is an explanatory view of the drive method which chooses a 2-pixel line as coincidence. In drawing 246, the condition that Pixels 16a and 16b are chosen is illustrated. TFT11of pixel 16a a and TFT11a of pixel 16b pass Current Idd to the source signal line 18, respectively.

[0609] In order to give explanation easy here, the current which TFT11a of each pixel passes presupposes that there is no variation, and is made into 2xIdd=Iw. That is, the source driver circuit 14 absorbs the current Iw from the source signal line 18, and is programmed by the capacitor 19 whose current which divided this current Iw into two equally is each pixel. For example, it is Iw=30nA if it is Idd=15nA.

[0610] Two write-in pixel lines 871 (871a, 871b) are chosen, and sequential selection is made the lower side from the surface of Screen 21 so that it may illustrate to drawing 247 (a). However, 871b is lost, although it writes in and pixel line 871a exists, if it comes to the lower side of a screen as shown in drawing 871 (b). That is, the pixel line only of one to choose is lost. Therefore, the current Iw impressed to the source signal line 18 is altogether written in pixel line 871a. Therefore, it will become Iw=Idd and a twice as many current as this will be programmed by the pixel as compared with pixel line 871a of drawing 247 (a).

[0611] To this technical problem, this invention forms the dummy pixel line 2471 the lower side of Screen 21 so that it may illustrate to drawing 247 (b) (arrangement). Therefore, when a selection pixel line is chosen to the lower side of Screen 21, the last pixel line and the dummy pixel line 2471 of Screen 21 are chosen. Therefore, the current of Idd=Iw/2 as a convention is written in the write-in pixel line of drawing 247 (b).

[0612] Drawing 248 shows the condition of drawing 247 (b). When a selection pixel line is chosen to the pixel 16b line of the lower side of Screen 21 so that clearly [in drawing 248], the last pixel line 2471 of Screen 21 is chosen. Moreover, the pixel line 2471 is formed so that it may illustrate to drawing 249 (arrangement). However, the dummy pixel line 2471 is arranged out of a viewing area 21. That is, or it does not switch on the light, the light is not made to switch on, or the dummy pixel line 2471 is constituted so that it may not be visible as a display, even if it switches on the light.

[0613] In addition, even if it is the configuration which forms the dummy pixel line 2471 as shown in drawing 248 and drawing 249 (arrangement), it cannot be overemphasized that gate signal line 17b etc. can be carried out in common with the lighting control line 1791 as drawing 179 explained, and a block lighting drive can be carried out. Moreover, it cannot be overemphasized that it is also combinable also with a reverse bias drive (refer to drawing 250).

[0614] Although [in drawing 247] the dummy pixel (line) 2471 is formed the lower side of Screen 21 (it forms and arranges), it does not limit to this. For example, when [which is scanned from the lower side of a screen to the surface] carrying out (vertical inversion scan), the dummy pixel line 2471 should be formed also in the surface of Screen 21 so that it may illustrate to drawing 251 (b), so that it may illustrate to drawing 251 (a). That is, the dummy pixel line 2471 is formed in each of the lower side for the surface of Screen 21 (refer to drawing 254). (arrangement) By constituting as mentioned above, it can respond now also to the vertical reversal scan of a screen.

[0615] The above example was the case where coincidence selection of the 2-pixel line was made. The method which does not limit to this and makes coincidence selection of the 5-pixel line is sufficient as this invention.

[0616] Drawing 255 is an explanatory view of the drive approach which chooses a 5-pixel line as coincidence. The dummy pixel line 2471 for 4 pixels is formed the vertical side of a screen so that it may illustrate to drawing 255.

[0617] Drawing 271 is an explanatory view of the drive approach of the display panel of drawing 255. From the source driver circuit 14, it explains that the current of Iw=5xIdd outputs (or absorption). Current Idd is a current (current programmed) written in each pixel. In addition, it cannot be overemphasized that Idd changes with display images.

[0618] By the drive method which chooses a 5-pixel line as coincidence, the source driver circuit 14 is outputted with a 5 times as many current as the current Idd written in a pixel. In drawing 271 (a), only the pixel on No. 1 of Screen 21 is chosen. However, in this condition, since it is Iw=5xIdd, a 5 times as many current as a predetermined value will write in, and it will be written in the pixel line 871.

[0619] To this technical problem, by this invention, dummy pixel line 2471a of a 4-pixel line is chosen as coincidence so that it may illustrate to drawing 271 (a). That is, coincidence

selection of the write-in pixel line 871 of four dummy pixel line 2471a and one viewing area is made. Therefore, since it is set to Iw=5xIdd, the predetermined current Idd is programmed by the pixel line 871 chosen in drawing 271 (a).

[0620] In drawing 271 (b), two write-in pixel lines 871 of a viewing area 21 are chosen, one is not chosen but, as for dummy pixel line 2471a, three are chosen. Therefore, the selected pixel line becomes a total of five. Therefore, since it is set to Iw=5xIdd, the predetermined current Idd is programmed by two pixel lines 871 chosen in drawing 271 (b).

[0621] Similarly, in drawing 271 (c), three write-in pixel lines 871 of a viewing area 21 are chosen, two are not chosen but, as for dummy pixel line 2471a, two are chosen. Therefore, the selected pixel line becomes a total of five. Therefore, since it is set to Iw=5xIdd, the predetermined current Idd is programmed by two pixel lines 871 chosen in drawing 271 (c).

[0622] As mentioned above, in drawing 271 (d), four write-in pixel lines 871 of a viewing area 21 are chosen, three are not chosen but, as for dummy pixel line 2471a, one is chosen. Moreover, in drawing 271 (e), five write-in pixel lines 871 of a viewing area 21 are chosen, and dummy pixel line 2471a is not chosen. As mentioned above, sequential selection of the five pixel lines is made (drawing 271 (f), (g), (h)). If it reaches the lower side of Screen 21, the selection number of dummy pixel line 2471b will increase to every 1H.

[0623] Even if the pixel line which makes coincidence selection by driving as mentioned above increases, in case the surface or the lower side of Screen 21 is chosen, the current value to which a pixel line including the dummy pixel line 2471 can be made into constant value, therefore the source driver circuit 14 outputs it can be fixed the coincidence selection drawing behavior twice of image data. Therefore, the configuration of the source driver circuit 14 becomes easy, and a target predetermined current (electrical potential difference) is written in each pixel.

[0624] As mentioned above, what is necessary is just to form 5-1=4 dummy pixel line in one side of a screen by the drive method which chooses a 5-pixel line as coincidence. That is, what is necessary is just to form or arrange the dummy pixel line more than the book (pixel line count -1) chosen as coincidence.

[0625] Moreover, the above examples were the example which makes coincidence selection of the 2-pixel line, and an example which makes coincidence selection of the 5-pixel line. This invention may not be limited to this and may choose a 3-pixel line or the pixel line beyond it as coincidence.

[0626] Moreover, in the above example, although explained having made coincidence selection of the adjoining pixel line, it does not limit to this. For example, you may choose every 1-pixel line and may choose at random.

[0627] In the above example, in case you choose two or more pixel lines, the dummy pixel line 2471 is chosen in the part of the beginning of a scan of Screen 21, or the last, and let the current Iw which flows to the source driver circuit 14 be constant value. of course, it is not limited to coming out and this invention making constant value the current which is what forms or arranges a dummy pixel line and which exists and flows to the source driver circuit 14.

[0628] Drawing 272 is the drive approach of making the period when write-in pixel line 871a is not chosen turning on dummy pixel line 2471a. Moreover, although write-in pixel line 871a is considering as the 1-pixel line, it does not limit to this, and it cannot be overemphasized that you may be two or more pixel line as shown in drawing 271. When performing such a drive, the case where the gate driver circuit 12 is directly formed [******] in the array substrate 49 (configuration with a built-in gate driver) is illustrated.

[0629] It is difficult from a viewpoint of the yield or formation area to form a complicated circuit with a configuration with a built-in gate driver. Therefore, the gate driver circuit 12 is formed by the circuitry simplified as much as possible. In order to simplify circuitry, the case

where the actuation has constraint generates the formed gate driver circuit 12.

[0630] For example, if it is not after 2-3 clock (a clock is set to 1H) even if it puts data (ST) into the shift register 22 of the gate driver circuit 12, it will be illustrated that an ON signal (Vgl) does not output to gate signal line 17a. However, after on-data are outputted to gate signal line 17a (1), synchronizing with the clock of 1H, the sequential shift of the on-data location is carried out henceforth.

[0631] As mentioned above, unless it is after 2-3 clock and gate signal line 17a (1) is chosen, any pixel line will be chosen between 2-3 clocks. As for the output of the source driver circuit 14, it is [this period] desirable to consider as zero (for there to be no I/O of a current) condition. However, the output stage of the source driver circuit 14 consists of current regulator circuits. Therefore, it is difficult to set the flowing current to 0 completely. If a current flows to the source signal line 18 (the source driver circuit 14 absorbs the charge of the source signal line 18), the potential of the source signal line 18 will be reduced. A fall of the potential of the source signal line 18 may also reduce the potential of the capacitor 19 of each pixel 16. If the potential of a capacitor 19 falls, since it will become in the direction in which the potential of the gate terminal of TFT11a is reduced, TFT11a becomes the direction which passes a current more. That this condition appears notably is the case where a screen is in a black display condition. When TFT11a of each pixel passes a current, it is because a black float is generated.

[0632] When which gate signal line 17 of a viewing area 21 is not chosen to this technical problem (condition), the dummy pixel line 2471 is chosen, and it drives so that a current may flow to a source signal line. That is, the switching TFT11 of the dummy pixel line 2471 is made to turn on, and the impedance of TFT11a for a drive is reduced. Therefore, the current which flows into the source driver circuit 14 is constituted so that it may be supplied from TFT11a of the dummy pixel line 2471.

[0633] Moreover, in the condition that, as for important one, neither of the pixel lines of a viewing area 21 is chosen, the output stage circuit of the source driver circuit 14 is considering as the condition of current OFF as much as possible.

[0634] In drawing 272 (a1), it assumes that the start signal was impressed to the shift register 22 of the circuit 12 with a built-in gate driver. Drawing 272 (a2) is after 1H as compared with drawing 272 (a1). the same -- drawing 272 (a3) -- further -- after 1H -- it is -- drawing 272 (a4) -- further -- it is after 1H.

[0635] In drawing 272 (a), neither of the gate signal lines of a viewing area 21 is chosen, but a pixel line (1) is chosen for the first time in drawing 272 (a3) after 3H, a 1-pixel line shift is carried out henceforth in drawing 272 (a4), and the first 2H period shows the place where the pixel line (2) was chosen.

[0636] Neither of the pixel lines is chosen in drawing 272 (a1) (a2). As the cure, dummy pixel line 2471a is chosen, and the current is supplied to dummy pixel line 2471a from TFT11a so that potential of the source signal line 18 may not be changed.

[0637] As mentioned above, by supplying a current from dummy pixel line 2471a, there is no black float and good image display can be realized. Moreover, change of the white balance of a screen etc. is not generated, either.

[0638] In addition, in drawing 272 (a), although dummy pixel line 2471a of the side near the source driver circuit 14 is chosen, it does not limit to this. For example, as shown in drawing 272 (b), dummy pixel line 2471b of a side far from the source driver 14 may be chosen. Moreover, both dummy pixel lines 2417a and 2471b may be chosen.

[0639] Moreover, drawing 272 (a) and the actuation of the drive method of drawing 272 (b) are the same. In drawing 272 (b1), a start signal is impressed to the shift register 22 of the circuit 12 with a built-in gate driver, and drawing 272 (b2) is after 1H as compared with drawing 272 (b1). the same -- drawing 272 (b3) -- further -- after 1H -- it is -- drawing 272

(b4) -- further -- it is after 1H.

[0640] Like drawing 272 (a) of drawing 272 (b), neither of the gate signal lines of a viewing area 21 is chosen, but a pixel line (1) is chosen for the first time in drawing 272 (b3) after 3H, a 1-pixel line shift is carried out henceforth in drawing 272 (b4), and the first 2H period shows the place where the pixel line (2) was chosen. As shown in drawing 272 (b), the way which chooses dummy pixel line 2471b of the one distant from the source driver circuit 14 tends to stabilize the potential of the source signal line 18. This condition is shown in drawing 253.

[0641] In addition, in the example of drawing 272, although the number of the pixel lines to choose was one, they are not limited to this. For example, it cannot be overemphasized that it is applicable also to the drive method which chooses two or more pixel lines as shown in drawing 271. In addition, in the drive method which chooses two or more pixel lines, if it aims at solving the black float generated when the pixel line of a viewing area 21 is not chosen at all, or an image quality change problem, as shown in drawing 271, it is not necessary to form two or more dummy pixel lines 2471. As illustrated to drawing 272, you may be one dummy pixel line 2471. It is because it is possible to stabilize the potential of the source signal line 18 etc. in this one dummy pixel line.

[0642] Moreover, the dummy pixel lines 2471a and 2471b may change the dummy pixel line 2471 to choose by the scanning direction (for example, drawing 247 and drawing 251) of Screen 21.

[0643] In drawing 272, the dummy pixel line 2471 was chosen in the condition that neither of the pixel lines of a viewing area 21 is chosen among the periods of one frame (or 1 field). However, the pixel line may not be chosen as 1 horizontal-scanning period in the real drive condition.

[0644] Drawing 252 is a wave form chart of operation for explaining this condition. In the display of this invention, the pixel line as which the pixel line was chosen and chosen with the clock of 1H (1 horizontal-scanning period) carries out the sequential shift. However, the pixel line is chosen as the predetermined period also in the period of 1H.

[0645] As for gate signal line 17b of the pixel line chosen fundamentally, OFF state voltage (Vgh) is impressed during the whole term of 1H. In drawing 252, OFF state voltage is impressed to gate signal line 17b of a pixel line (1) at the time of the pixel line number 1. Moreover, OFF state voltage is impressed to gate signal line 17b of a pixel line (2) at the time of the pixel line number 2.

[0646] On the other hand, as for gate signal line 17a, the selection electrical potential difference (Vgl) is impressed to the period shorter than 1H. Therefore, a pixel line (1) does not choose the period of a, and the period of b at the time of the pixel line number 1. To run and it is easy to generate an electrical potential difference to generate a non-choosing period as mentioned above, when the timing from which gate signal line 17b changes, and the timing from which gate signal line 17a changes are in agreement. It is because the electrical potential difference (current) of a request to a capacitor 19 will no longer be held and variation will occur in the luminescence brightness of EL element 15, if it runs and an electrical potential difference occurs.

[0647] As for the period of a at least shown in drawing 252, securing is desirable. Depending on the case, 0 is sufficient as the period of b. This should just determine EL element 15 in consideration of the timing which carries out on-off control. It is desirable to choose gate signal line 17a from the timing to which gate signal line 17b changed from Vgl to Vgh (that is, condition of not choosing) at least, fundamentally, after one eighth of 1H passes below time amount 1/64 of beyond the time amount of 1H. Furthermore, preferably, after one eighth of 1H passes below time amount 1/32 of beyond the time amount of 1H, it is desirable to choose gate signal line 17a. Or it is desirable to choose gate signal line 17a from the timing to

which gate signal line 17b changed from Vgl to Vgh (that is, condition of not choosing) at least, after passing below 20microsec more than 0.5microsec. Furthermore, preferably, after passing below 10microsec more than 1microsec, it is desirable to choose gate signal line 17a. Moreover, it is still more desirable, when it constitutes so that the precharge (discharge) electrical potential difference explained by drawing 52 etc. may be impressed to the period of this a, or the period of b.

[0648] The change signal CSW which illustrates the period when gate signal line 17a is chosen to drawing 252 serves as Vgh. The output stage of the source driver 14 is controlled by Vgl level of this change signal CSW to be in an OFF state. Moreover, it is controlled by Vgl level of this change signal CSW so that the dummy pixel line 2471 explained in drawing 272 is chosen. By making it constitute or operate as mentioned above, there is no black float and good image display can be realized. Moreover, it can avoid also generating change of the white balance of a screen etc.

[0649] In addition, in drawing 253, although the dummy pixel 2471 was illustrated as EL element 15 and TFT11d were formed, the dummy pixel 2471 supplies fundamentally the current passed to the source signal line 18 (depending on a pixel configuration, a current is absorbed from the source signal line 18). Therefore, EL element 15 does not have the need. Conversely, if EL element 15 etc. is formed, EL element 15 will light up and it will become about a problem.

[0650] This invention does not form EL element 15 etc. so that the dummy pixel 2471 may be illustrated to drawing 258. It runs, and even if capacitor 19b for electrical-potential-difference generating adds, it is not necessary to carry out it. However, when it runs in the pixel of a viewing area 21 and capacitor 19b for electrical-potential-difference generating is formed, forming also in the dummy pixel 2471 is desirable. It is for making it equal to the current on which TFT11a of the pixel 16 of a viewing area 21 passes the current which TFT11a of the dummy pixel 2471 passes.

[0651] Drawing 258 is the case of the pixel configuration of drawing 1. In the dummy pixel 2471, TFT11b for a drive and EL element 15 are deleted so that it may illustrate to drawing 259 with the pixel configuration of drawing 21, drawing 43, and the current mirror of drawing 71. In the pixel configuration of electrical-potential-difference programs, such as drawing 54, drawing 67, and drawing 103, it constitutes from TFT11b and capacitor 19a for switching so that it may illustrate to drawing 260. In an electrical-potential-difference program method, it is because a current is not supplied to the source signal line 18 from TFT for a drive of a pixel.

[0652] The dummy pixel 2471 illustrated to drawing 258, drawing 259, etc. does not need to emit light. Therefore, EL film is not formed in the pixel electrode 48 of the dummy pixel 2471 so that it may illustrate to drawing 256. An insulator layer 2561 is formed in the pixel electrode 48 so that it may illustrate to drawing 256, and it considers as an insulating condition. Or the pixel electrode 48 of the dummy pixel 2471 and the metal membrane of a cathode 46 are electrically changed into a short circuit condition so that it may illustrate to drawing 257. Thus, the potential of the pixel electrode 48 is stabilized by constituting.

[0653] If a frame rate is low like drawing 136 when one viewing area 311 moves to down from on a screen, as shown in drawing 141, it will be recognized visually that a viewing area 311 moves. It becomes that it is easy to be recognized when a palpebra is closed especially, or when moving a face up and down.

[0654] It is good to divide a viewing area 311 into plurality so that it may illustrate to drawing 142 to this technical problem. Drawing 142 (b) is dividing the non-display field 312 into three. If the part which added these three serves as area of S (N-1)/N, it will become the brightness and the EQC of drawing 141.

[0655] Drawing 143 is a voltage waveform impressed to the gate signal line 17. The

difference between drawing 140 and drawing 143 is actuation of gate signal line 17b fundamentally. Gate signal line 17b carries out on-off (Vgl and Vgh) actuation by the number corresponding to the number which divides a screen. other points are almost the same as that of drawing 140 -- or since it can guess, explanation is omitted.

[0656] In addition, the scanning direction of the astigmatism LGT viewing area 312 is not limited only to down from on a screen so that it may illustrate to drawing 142 (b). You may scan above from under a screen. moreover, the scanning direction from a top to the bottom and the scanning direction from the bottom to above -- alternation -- or you may scan at random. Moreover, it cannot be overemphasized that the number of partitions may be changed in the predetermined location of every frame and the display screen 21.

[0657] As mentioned above, a flicker of a screen decreases by dividing a viewing area 311 into plurality. Therefore, there is no generating of a flicker and it can realize good image display. In addition, division may be made finer. However, the more it divides, the more a flicker is mitigated. Since especially the responsibility of EL element 15 is quick, even if it turns on and off by time amount smaller than 5microsec, there is no fall of display brightness.

[0658] In the drive approach of this invention, turning on and off of EL element 15 is controllable by turning on and off of the signal impressed to gate signal line 17b. Therefore, a clock frequency is controllable by the low frequency of KHz order. Moreover, an image memory etc. is not needed although black screen insertion (non-display field 312 insertion) is realized. Therefore, the drive circuit or approach of this invention is realizable by low cost.

[0659] Drawing 144 is the case where the pixel line chosen as coincidence is a 2-pixel line. According to the examined result, the approach of choosing a 2-pixel line as coincidence in the display panel formed with the low-temperature polish recon technique had practical display homogeneity. This is presumed because the property of TFT11a for a drive of the pixel which adjoined is extremely in agreement. Moreover, when carrying out laser annealing, the good result was obtained by irradiating the direction of radiation of stripe-like laser in parallel with the source signal line 18.

[0660] In drawing 144, when a write-in pixel line is eye (1) pixel line, as for gate signal line 17a, (1) and (2) are chosen (refer to drawing 145). That is, switching TFT11b of a pixel line (1) and (2) and TFT11c are ON states. Moreover, gate signal line 17b is the opposite phase of gate signal line 17a. Therefore, the current is not flowing to EL element 15 of the pixel line which switching TFT11d of a pixel line (1) and (2) is an OFF state at least, and corresponds. That is, it is in the astigmatism LGT condition 312. In addition, in drawing 144, in order to reduce generating of a flicker, the viewing area 311 is divided into five.

[0661] Ideally, 2 pixels (line) TFT11a passes the current of Idx5 (in the case of N= 10) to the source signal line 18, respectively. And a 5 times as many current as this is programmed by the capacitor 19 of each pixel 16.

[0662] Since the pixel line chosen as coincidence is a 2-pixel line (K= 2), two drive TFT11a operates. That is, per pixel, and 10 / 2= 5 times as many current as this flows to TFT11a. In the source signal line 18, the current which added two program currents of TFT11a flows.

[0663] For example, originally, it considers as the current Id to write in and the current of Idx10 is passed to the source signal line 18 at write-in pixel line 871a. Since the image data of normal is written in behind, write-in pixel line 871b is satisfactory. Pixel line 871b is the same display as 871a between 1H periods. Therefore, pixel line 871b chosen in order to make write-in pixel line 871a and a current increase is made into the non-display condition 312 at least.

[0664] After the following 1H, gate signal line 17a (1) is un-choosing, and ON state voltage (Vgl) is impressed to gate signal line 17b. Moreover, gate signal line 17a (3) is chosen as coincidence (Vgl electrical potential difference), and a program current flows from TFT11a of the selected pixel line (3) to the source signal line 18 toward the source driver 14. Thus,

from that of operating, the image data of normal is held at a pixel line (1).

[0665] After the following 1H, gate signal line 17a (2) is un-choosing, and ON state voltage (Vgl) is impressed to gate signal line 17b. Moreover, gate signal line 17a (4) is chosen as coincidence (Vgl electrical potential difference), and a program current flows from TFT11a of the selected pixel line (4) to the source signal line 18 toward the source driver 14. Thus, from that of operating, the image data of normal is held at a pixel line (2). one screen is rewritten by scanning, shifting a 1-pixel line every with the above actuation.

[0666] Although it is the same as that of drawing 40, in order to program with a 5 times as many current (electrical potential difference) as this to each pixel, by the drive approach of drawing 149, the luminescence brightness of EL element 15 of each pixel becomes 5 times ideally. Therefore, the brightness of a viewing area 311 becomes 5 times from a predetermined value. What is necessary is just to let one fifth of the range of the display screen 1 be the non-display fields 312, including the write-in pixel line 871 so that you may illustrate to drawing 87 in order to make this into predetermined brightness. Since this was explained using drawing 137 etc., it omits explanation.

[0667] The animation display engine performance improves, so that area of the black viewing area (non-display field) 312 occupied to the display screen 21 is enlarged. Therefore, what is necessary is to lessen the non-display field 311 so that it may illustrate to drawing 141, and just to enlarge area of the non-display field 312.

[0668] By the drive approach which chooses two or more pixel lines as coincidence, it becomes difficult to absorb the property variation of TFT11a, so that the pixel line count chosen as coincidence increases. However, when a selection number falls, the current programmed to 1 pixel becomes large, and a big current will be passed to EL element 15. If the current passed to EL element 15 is large, EL element 15 will become easy to deteriorate.

[0669] Drawing 146 solves this technical problem. As the fundamental concept of drawing 146 explained 1/2H (1/2 of a horizontal scanning period) by drawing 88, two or more pixel lines are chosen as coincidence, and 1/2H (1/2 of a horizontal scanning period) of after that combine the approach of choosing a 1-pixel line, as drawing 134 explained. Thus, by constructing and uniting, the property variation of TFT11a can be absorbed and homogeneity within a field can be made good more at high speed.

[0670] In drawing 146, in order to give explanation easy, by the 1st period, a 5-pixel line is chosen as coincidence, and in the 2nd period, it explains noting that a 1-pixel line is chosen.

[0671] First, in the 1st period, a 5-pixel line is chosen as coincidence so that it may illustrate to drawing 146 (a1). This actuation was explained using drawing 88. The current passed to a source signal line is made into 25 times of a predetermined value. Therefore, a 5 times as many current as this is programmed by TFT11a of each pixel 16. Since it is a 25 times as many current as this, the charge and discharge of the parasitic capacitance 404 are carried out extremely for a short period of time. Therefore, the potential of a source signal line turns into target potential for a short time, and it is programmed so that the terminal voltage of the capacitor 19 of each pixel 16 also passes a current 5 times. Impression time amount of a current is set to 1/2H (1/2 of 1 horizontal-scanning period) these 25 times.

[0672] Since, as for the 5-pixel line of a write-in pixel line, the same image data is written in with a natural thing, let TFT11 be an OFF state so that you may not display. Therefore, a display condition serves as drawing 146 (a2).

[0673] The 1/2H next period chooses a 1-pixel line, and performs a current (electrical potential difference) program. This condition is illustrated to drawing 146 (b1). The current (electrical potential difference) program of the write-in pixel line 871a is carried out so that a 5 times as many current as this may be passed like the point. The current passed to each pixel in drawing 146 (a1) and drawing 146 (b1) is made the same, because change of the terminal voltage of the programmed capacitor 19 is made small and a target current can be passed

more at a high speed.

[0674] That is, it brings close in drawing 146 (a1) to the value to which a sink flows to two or more pixels, and the current of an outline flows a current at a high speed. In this 1st phase, since it is programming by two or more TFT11a, the error by the variation in TFT has occurred to desired value. Only the pixel line which writes in and holds data in the 2nd next phase is chosen, and a perfect program is performed from the desired value of an outline to predetermined desired value.

[0675] In addition, since it is the same as that of the example of drawing 87, drawing 88, drawing 134, etc. to scan the astigmatism LGT field 312 down from on a screen, and to scan write-in pixel line 871a down from on a screen, explanation is omitted.

[0676] Drawing 147 is a drive wave for realizing the drive approach of drawing 146. As shown in drawing 146, 1H (1 horizontal-scanning period) consist of two phases. These two phases are changed by the ISEL signal. The ISEL signal is illustrated to drawing 148.

[0677] First, the ISEL signal is explained. In drawing 148, the current output circuit 1222 consists of two, 1222a and 1222b. Each current output circuit 1222 consists of the DA circuits 1226, the OPEN amplifier 1224, etc. which carry out the DA translation of the 8-bit gradation data. Since circuit actuation of this current output circuit 1222 was explained above, it omits. Current output circuit 1222a consists of examples of 146 so that a 25 times as many current as this may be outputted. On the other hand, current output circuit 1222b is constituted so that a 5 times as many current as this may be outputted. A switching circuit 1223 is controlled by the ISEL signal, and the output of the current output circuits 1222a and 1221b is impressed to the source signal line 18.

[0678] Current output circuit 1222a to which an ISEL signal outputs a current 25 times at the time of L level is chosen, and the source driver IC 14 absorbs the current from the source signal line 18. At the time of H level, current output circuit 1222b which outputs a current 5 times is chosen, and the source driver IC 14 absorbs the current from the source signal line 18. Magnitude modification of currents, such as 25 times and 5 times, is easy. the value of resistance 1228 is changed -- being sufficient -- since -- it is . Moreover, it connects with making resistance 1228 into BORIUMU, or two or more resistance and an analog switch, and can change easily by choosing.

[0679] It writes in, as shown in drawing 147, and when a pixel line is eye (1) pixel line (see the column of the pixel line number 1 of drawing 147), as for gate signal line 17a, (1), (2), (3), (4), and (5) are chosen. That is, switching TFT11b of a pixel line (1), (2), (3), (4), and (5) and TFT11c are ON states. Moreover, since ISEL is L level, current output circuit 1222a which outputs a current 25 times is chosen, and it connects with the source signal line 18. Moreover, OFF state voltage (Vgh) is impressed to gate signal line 17b. Therefore, the current is not flowing to EL element 15 of the pixel line which switching TFT11d of a pixel line (1), (2), (3), (4), and (5) is an OFF state, and corresponds. That is, it is in the astigmatism LGT condition 312.

[0680] Ideally, 5-pixel TFT11a passes the current of Idx2 to the source signal line 18, respectively. And a 5 times as many current as this is programmed by the capacitor 19 of each pixel 16. Here, in order to make an understanding easy, it explains noting that the property (Vt, S value) of each TFT11a corresponds.

[0681] Since the pixel line chosen as coincidence is a 5-pixel line (K= 5), five drive TFT11a operates. That is, per pixel, and 25 / 5= 5 times as many current as this flows to TFT11a. In the source signal line 18, the current which added five program currents of TFT11a flows. For example, originally, it considers as the current Id to write in and the current of Idx25 is passed to the source signal line 18 at write-in pixel line 871a. In order to make the amount of currents to the write-in pixel line 871b source signal line 18 which writes in image data henceforth increase from a write-in pixel line (1), it is the pixel line used auxiliary. However,

since the image data of normal is written in behind, write-in pixel line 871b is satisfactory.

[0682] Therefore, pixel line 871b is the same display as 871a between 1H periods. Therefore, pixel line 871b chosen in order to make write-in pixel line 871a and a current increase is made into the non-display condition 312 at least.

[0683] In the following 1/2H (1/2 of a horizontal scanning period), only write-in pixel line 871a is chosen. That is, only eye (1) pixel line is chosen. ON state voltage (Vgl) is impressed for gate signal line 17a (1), and, as for gate signal line 17a (2), (3), (4), and (5), OFF (Vgh) is impressed so that clearly [in drawing 147]. Therefore, although TFT11a of a pixel line (1) is operating state (condition which supplies the current to the source signal line 18), switching TFT11b of a pixel line (2), (3), (4), and (5) and TFT11c are OFF states. That is, it is in the condition of not choosing. Moreover, since ISEL is H level, current output circuit 1222b which outputs a current 5 times is chosen, and this current output circuit 1222b and the source signal line 18 are connected. Moreover, the condition of gate signal line 17b does not have the previous condition of 1/2H, and change, and OFF state voltage (Vgh) is impressed. Therefore, the current is not flowing to EL element 15 of the pixel line which switching TFT11d of a pixel line (1), (2), (3), (4), and (5) is an OFF state, and corresponds. That is, it is in the astigmatism LGT condition 312.

[0684] From the above thing, TFT11a of a pixel line (1) passes the current of Idx5 to the source signal line 18, respectively. And a 5 times as many current as this is programmed by the capacitor 19 of each pixel line (1).

[0685] In the next horizontal scanning period, a 1-pixel line and a write-in pixel line shift. That is, a write-in pixel line is (2) shortly. In the first period of 1/2H, it writes in, as shown in drawing 147, and when a pixel line is eye (2) pixel lines, as for gate signal line 17a, (2), (3), (4), (5), and (6) are chosen. That is, switching TFT11b of a pixel line (2), (3), (4), (5), and (6) and TFT11c are ON states. Moreover, since ISEL is L level, current output circuit 1222a which outputs a current 25 times is chosen, and it connects with the source signal line 18. Moreover, OFF state voltage (Vgh) is impressed to gate signal line 17b. Therefore, the current is not flowing to EL element 15 of the pixel line which switching TFT11d of a pixel line (2), (3), (4), (5), and (6) is an OFF state, and corresponds. That is, it is in the astigmatism LGT condition 312. On the other hand, since the Vgl electrical potential difference is impressed, TFT11d is an ON state and gate signal line 17of pixel line (1) b (1) turns on EL element 15 of a pixel line (1).

[0686] Since the pixel line chosen as coincidence is a 5-pixel line (K= 5), five drive TFT11a operates. That is, per pixel, and 25 / 5= 5 times as many current as this flows to TFT11a. In the source signal line 18, the current which added five program currents of TFT11a flows.

[0687] In the following 1/2H (1/2 of a horizontal scanning period), only write-in pixel line 871a is chosen. That is, only eye (2) pixel lines is chosen. ON state voltage (Vgl) is impressed for gate signal line 17a (2), and, as for gate signal line 17a (3), (4), (5), and (6), OFF (Vgh) is impressed so that clearly [in drawing 147]. Therefore, although TFT11a of a pixel line (1) and (2) is operating state (condition that in the pixel line (1) supply a current to EL element 15 and the sink and the pixel line (2) supply the current to the source signal line 18), switching TFT11b of a pixel line (3), (4), (5), and (6) and TFT11c are OFF states. That is, it is in the condition of not choosing. Moreover, since ISEL is H level, current output circuit 1222b which outputs a current 5 times is chosen, and this current output circuit 1222b and the source signal line 18 are connected. Moreover, the condition of gate signal line 17b does not have the previous condition of 1/2H, and change, and OFF state voltage (Vgh) is impressed. Therefore, the current is not flowing to EL element 15 of the pixel line which switching TFT11d of a pixel line (2), (3), (4), (5), and (6) is an OFF state, and corresponds. That is, it is in the astigmatism LGT condition 312.

[0688] From the above thing, TFT11a of a pixel line (2) passes the current of Idx5 to the

source signal line 18, respectively. And a 5 times as many current as this is programmed by the capacitor 19 of each pixel line (2). One screen can be displayed by carrying out the above actuation one by one.

[0689] The drive approach explained in drawing 146 chooses a G pixel line (G is two or more) in the 1st period, and programs it in each pixel line to pass a N times as many current as this. It is the method programmed to choose a B pixel line (for it to be smaller than G and for B to be one or more) in the 2nd period after the 1st period, and to pass a N times as many current as this to a pixel.

[0690] However, there are other policies. A G pixel line (G is two or more) is chosen in the 1st period, and it programs so that the total current of each pixel line turns into a N times as many current as this. It is the method programmed so that a B pixel line (it is smaller than G and B is one or more) is chosen in the 2nd period after the 1st period and the current (current of a 1-pixel line when [however,] a selection pixel line is 1) of total of the selected pixel line becomes N times. For example, in drawing 146 (a1), a 5-pixel line is chosen as coincidence and a twice as many current as this is passed to TFT11a of each pixel. Therefore, to the source signal line 18, a 5x2 times = 10 times as many current as this flows. In the 2nd next period, a 1-pixel line is chosen in drawing 146 (b1). To 1 pixel this TFT11a, a 10 times as many current as this is passed.

[0691] If it is this method, as shown in drawing 148, two or more current output circuits 1222 are not required. Therefore, the source driver IC 14 can consist of one current output circuit 1222 in each source signal line.

[0692] That is, the output current of the source driver IC 14 which passes the current of the source signal line 18 by this method is constant value (naturally this constant value changes with image data.). in this case, it is not based on the number of selection pixels during 1H period, but is the semantics of being fixed -- it is . Therefore, the configuration of the source driver IC 14 becomes easy.

[0693] In addition, in drawing 146, although the period which chooses two or more pixel lines as coincidence was set to 1/2H and the period which chooses a 1-pixel line was set to 1/2H, it does not limit to this. It is good also considering the period which sets to 1/4H the period which chooses two or more pixel lines as coincidence, and chooses a 1-pixel line as 3/4H. Moreover, although the period which added the period which chooses two or more pixel lines as coincidence, and the period which chooses a 1-pixel line was set to 1H, it is not limited to this. For example, you may be 1.5H period also in 2H period.

[0694] Moreover, in drawing 146, though the period which chooses a 5-pixel line as coincidence is set to 1/2H and a 2-pixel line is chosen as coincidence in the 2nd next period, it is good. Even in this case, convenient image display is realizable practically.

[0695] Moreover, in drawing 146, although considered as two steps which set to 1/2H the 1st period which chooses a 5-pixel line as coincidence, and set to 1/2H the 2nd period which chooses a 1-pixel line, it does not limit to this. For example, it is good also as three phases which the 1st phase chooses a 5-pixel line as coincidence, and the 2nd period chooses a 2-pixel line among said 5-pixel lines, and finally choose a 1-pixel line. That is, you may also write image data in a pixel line in two or more phases.

[0696] In drawing 148, it was presupposed that two current output circuits 1222 are established in each source signal line 18. This is for outputting a 5 times as many current as this to outputting a 25 times as many current as this to the 1st period which is the 1st example of drawing 146, and the 2nd period.

[0697] In order to realize this in one current output circuit 1222, it is good to adopt the circuitry of drawing 149. The DA circuit 1224 carries out digital to analog by making magnitude of a reference electrical potential difference (Iref) into maximum. For example, if an Iref electrical potential difference is 5 (V), analog output of what divided 5 (V) into 256

will be carried out as the minimum value. that is, the maximum of analog output -- a 5(V)-1 bit analog value -- it is -- the minimum value -- 0 (V) -- it is -- min -- resolving power is 5 (V)/256 (when an input is a 8-bit specification). If an Iref electrical potential difference is 2.5 (V), analog output of what divided 2.5 (V) into 256 will be carried out as the minimum value. that is, the maximum of analog output -- a 2.5(V)-1 bit analog value -- it is -- the minimum value -- 0 (V) -- it is -- min -- resolving power is 2.5 (V)/256 (when an input is a 8-bit specification).

[0698] That is, an output current value can be changed by changing Iref dynamically in one current output circuit 1222. Drawing 149 is the implementation circuit.

[0699] In drawing 149, the resistance RI which quadrisects Vi electrical potential difference is formed. This electrical potential difference by which the partial pressure was carried out is inputted into a switching circuit 1223, one electrical potential difference is chosen, and it becomes an Iref electrical potential difference. This Iref electrical potential difference is inputted into DA converter 1224. Therefore, the scale factor of the output current can be changed from that of changing the current output circuit 1222 where the Iref electrical potential difference of the period of 1/2H of the first half and the Iref electrical potential difference of the period of 1/2H of the second half were connected to all the source signal lines 18.

[0700] Of course, it cannot be overemphasized that an Iref electrical potential difference may be generated by selection of two or more DA circuits 1224 so that it may illustrate to drawing 150.

[0701] Also in drawing 148, the lighting viewing area 311 is good also as one so that it may illustrate to drawing 151. Moreover, you may divide into two or more lighting viewing areas 311 so that it may illustrate to drawing 152.

[0702] As illustrated to drawing 153, when a write-in pixel line is eye (1) pixel line, as for gate signal line 17a, (1), (2), (3), (4), and (5) are chosen. That is, switching TFT11b of a pixel line (1), (2), (3), (4), and (5) and TFT11c are ON states. Moreover, since ISEL is L level, current output circuit 1222a which outputs a current 25 times is chosen, and it connects with the source signal line 18. Moreover, OFF state voltage (Vgh) is impressed to gate signal line 17b. Therefore, the current is not flowing to EL element 15 of the pixel line which switching TFT11d of a pixel line (1), (2), (3), (4), and (5) is an OFF state, and corresponds. That is, it is in the astigmatism LGT condition 312.

[0703] Since the pixel line chosen as coincidence is a 5-pixel line (K= 5), five drive TFT11a operates. That is, per pixel, and 25 / 5= 5 times as many current as this flows to TFT11a. In the source signal line 18, the current which added five program currents of TFT11a flows. For example, originally, it considers as the current Id to write in and the current of Idx25 is passed to the source signal line 18 at write-in pixel line 871a. In order to make the amount of currents to the write-in pixel line 871b source signal line 18 which writes in image data henceforth increase from a write-in pixel line (1), it is the pixel line used auxiliary. However, since the image data of normal is written in behind, write-in pixel line 871b is satisfactory.

[0704] Therefore, pixel line 871b is the same display as 871a between 1H periods. Therefore, pixel line 871b chosen in order to make write-in pixel line 871a and a current increase is made into the non-display condition 312 at least.

[0705] In the following 1/2H (1/2 of a horizontal scanning period), only write-in pixel line 871a is chosen. That is, only eye (1) pixel line is chosen. ON state voltage (Vgl) is impressed for gate signal line 17a (1), and, as for gate signal line 17a (2), (3), (4), and (5), OFF (Vgh) is impressed. Therefore, although TFT11a of a pixel line (1) is operating state (condition which supplies the current to the source signal line 18), switching TFT11b of a pixel line (2), (3), (4), and (5) and TFT11c are OFF states. That is, it is in the condition of not choosing. Moreover, since ISEL is H level, current output circuit 1222b which outputs a current 5 times is chosen,

and this current output circuit 1222b and the source signal line 18 are connected. Moreover, the condition of gate signal line 17b does not have the previous condition of 1/2H, and change, and OFF state voltage (Vgh) is impressed. Therefore, the current is not flowing to EL element 15 of the pixel line which switching TFT11d of a pixel line (1), (2), (3), (4), and (5) is an OFF state, and corresponds. That is, it is in the astigmatism LGT condition 312.

[0706] From the above thing, TFT11a of a pixel line (1) passes the current of Idx5 to the source signal line 18, respectively. And a 5 times as many current as this is programmed by the capacitor 19 of each pixel line (1).

[0707] In the next horizontal scanning period, a 1-pixel line and a write-in pixel line shift. That is, a write-in pixel line is (2) shortly. In the first period of 1/2H, when it is eye (2) pixel lines, as for gate signal line 17a, (2), (3), (4), (5), and (6) are chosen. That is, switching TFT11b of a pixel line (2), (3), (4), (5), and (6) and TFT11c are ON states. Moreover, since ISEL is L level, current output circuit 1222a which outputs a current 25 times is chosen, and it connects with the source signal line 18. Moreover, OFF state voltage (Vgh) is impressed to gate signal line 17b. Therefore, the current is not flowing to EL element 15 of the pixel line which switching TFT11d of a pixel line (2), (3), (4), (5), and (6) is an OFF state, and corresponds. That is, it is in the astigmatism LGT condition 312. On the other hand, since the Vgl electrical potential difference is impressed, TFT11d is an ON state and gate signal line 17of pixel line (1) b (1) turns on EL element 15 of a pixel line (1).

[0708] Since the pixel line chosen as coincidence is a 5-pixel line (K= 5), five drive TFT11a operates. That is, per pixel, and 25 / 5= 5 times as many current as this flows to TFT11a. In the source signal line 18, the current which added five program currents of TFT11a flows.

[0709] In the following 1/2H (1/2 of a horizontal scanning period), only write-in pixel line 871a is chosen. That is, only eye (2) pixel lines is chosen. ON state voltage (Vgl) is impressed for gate signal line 17a (2), and, as for gate signal line 17a (3), (4), (5), and (6), OFF (Vgh) is impressed. Therefore, although TFT11a of a pixel line (1) and (2) is operating state (condition that in the pixel line (1) supply a current to EL element 15 and the sink and the pixel line (2) supply the current to the source signal line 18), switching TFT11b of a pixel line (3), (4), (5), and (6) and TFT11c are OFF states. That is, it is in the condition of not choosing. Moreover, since ISEL is H level, current output circuit 1222b which outputs a current 5 times is chosen, and this current output circuit 1222b and the source signal line 18 are connected. Moreover, the condition of gate signal line 17b does not have the previous condition of 1/2H, and change, and OFF state voltage (Vgh) is impressed. Therefore, the current is not flowing to EL element 15 of the pixel line which switching TFT11d of a pixel line (2), (3), (4), (5), and (6) is an OFF state, and corresponds. That is, it is in the astigmatism LGT condition 312.

[0710] From the above thing, TFT11a of a pixel line (2) passes the current of Idx5 to the source signal line 18, respectively. And a 5 times as many current as this is programmed by the capacitor 19 of each pixel line (2). One screen can be displayed by carrying out the above actuation one by one.

[0711] Although the above explanation is also clear, the above actuation is the same as that of drawing 147. A difference is actuation of gate signal line 17b. Gate signal line 17b carries out on-off (Vgl and Vgh) actuation by the number corresponding to the number which divides a screen.

[0712] In addition, the scanning direction of the astigmatism LGT viewing area 312 is not limited only to down from on a screen so that it may illustrate also to drawing 152. You may scan above from under a screen. moreover, the scanning direction from a top to the bottom and the scanning direction from the bottom to above -- alternation -- or you may scan at random. Moreover, it cannot be overemphasized that the number of partitions may be changed in the predetermined location of every frame and the display screen 21.

[0713] As mentioned above, a flicker of a screen decreases by dividing a viewing area 311 into plurality. Therefore, there is no generating of a flicker and it can realize good image display. In addition, division may be made finer. However, the more it divides, the more a flicker is mitigated. Since especially the responsibility of EL element 15 is quick, even if it turns on and off by time amount smaller than 5microsec, there is no fall of display brightness.

[0714] The G pixel line (G is two or more) was chosen in the 1st period, and it programmed to pass a N times as many current as this in each pixel line, and in the 2nd period after the 1st period, the B pixel line (it is smaller than G and B is one or more) was chosen, and the example of drawing 153 was also made into the method programmed to pass a N times as many current as this to a pixel. However, there are other policies as well as drawing 147. That is, a G pixel line (G is two or more) is chosen in the 1st period, and it programs so that the total current of each pixel line turns into a N times as many current as this. It is the method programmed so that a B pixel line (it is smaller than G and B is one or more) is chosen in the 2nd period after the 1st period and the current (current of a 1-pixel line when [however,] a selection pixel line is 1) of total of the selected pixel line becomes N times.

[0715] The above example was the approach of displaying an image by sequential scanning. That is, if it says with a TV signal, it will be a non-interlaced drive (progressive drive). This invention is effective also in an interlace drive. Drawing 154 is an explanatory view of an interlace drive.

[0716] In addition, an interlace drive is usually one frame in the 2 fields. The 2 fields also explained drawing 154 as one frame (one screen). However, this is the case of the TV signal of NTSC and does not necessarily need to keep a 2 field =1 frame principle in image display, such as a cellular phone.

[0717] For example, it is good also as one frame in the 4 field. The 1st field writes in a 4Y-3 (Y is zero or more integers) pixel line, and the 2nd field writes in a 4Y-2 (Y is zero or more integers) pixel line. The 3rd field writes in a 4Y-1 (Y is zero or more integers) pixel line, and the 4th field is a method which writes in 4Y (Y is zero or more integers) pixel line. That is, an interlace drive is the approach of constituting one frame (one screen) from two or more fields.

[0718] Drawing 154 (a) is the 1st field and writes in an even-pixel line. Drawing 154 (b) writes in the odd-pixel line which is the 2nd field. Drawing 155 is a drive wave for realizing the drive approach of drawing 154. In addition, the odd number field and the even number field are the things on expedient. Drawing 154 explains first writing in an image from an odd-pixel line.

[0719] In drawing 154, gate signal line 17a (1) is chosen (Vgl electrical potential difference), and a program current flows from TFT11a of the selected pixel line to the source signal line 18 toward the source driver 14. Here, in order to give explanation easy, it explains first that write-in pixel line 871a is eye pixel line (1) watch.

[0720] Moreover, the program current which flows to the source signal line 18 is N times (in order to give explanation easy, it explains as N= 10 like an old example.) of a predetermined value. In addition, it does not limit to N= 10. of course, since a predetermined value is a data current which displays an image, unless it is white raster display etc., it is not a fixed value. it is .

[0721] When a write-in pixel line is eye (1) pixel line, the Vgl electrical potential difference is impressed to gate signal line 17a (1). Switching TFT11b and TFT11c are ON states. Moreover, the Vgh electrical potential difference is impressed to gate signal line 17b (1). Therefore, the current is not flowing to EL element 15 of the pixel line which switching TFT11d of a pixel line (1) is an OFF state, and corresponds. That is, it is in the astigmatism LGT condition 312.

[0722] A write-in pixel line is eye (3) pixel lines the following 1H. The Vgl electrical potential difference is impressed to gate signal line 17a (3). Switching TFT11b and TFT11c

are ON states. Moreover, the Vgh electrical potential difference is impressed to gate signal line 17b (3). Therefore, the current is not flowing to EL element 15 of the pixel line which switching TFT11d of a pixel line (3) is an OFF state, and corresponds. That is, it is in the astigmatism LGT condition 312. The Vgl electrical potential difference is impressed to gate signal line 17b (1). Switching TFT11d is an ON state. Therefore, switching TFT11d of a pixel line (1) is an ON state, and EL element 15 of a corresponding pixel line emits light.

[0723] A write-in pixel line is eye (5) pixel lines the following 1H. The Vgl electrical potential difference is impressed to gate signal line 17a (5). Switching TFT11b and TFT11c are ON states. Moreover, the Vgh electrical potential difference is impressed to gate signal line 17b (5). Therefore, the current is not flowing to EL element 15 of the pixel line which switching TFT11d of a pixel line (5) is an OFF state, and corresponds. That is, it is in the astigmatism LGT condition 312. The Vgl electrical potential difference is impressed to gate signal line 17b (3). Switching TFT11d is an ON state. Therefore, switching TFT11d of a pixel line (3) is an ON state, and EL element 15 of a corresponding pixel line emits light.

[0724] As mentioned above, sequential selection of the odd-pixel line is made, and image data is written and crowded with the 1st field.

[0725] In the 2nd field, image data is written in one by one from eye (2) pixel lines. The Vgl electrical potential difference is impressed to gate signal line 17a (2). Switching TFT11b and TFT11c are ON states. Moreover, the Vgh electrical potential difference is impressed to gate signal line 17b (2). Therefore, the current is not flowing to EL element 15 of the pixel line which switching TFT11d of a pixel line (2) is an OFF state, and corresponds. That is, it is in the astigmatism LGT condition 312.

[0726] A write-in pixel line is eye (4) pixel lines the following 1H. The Vgl electrical potential difference is impressed to gate signal line 17a (4). Switching TFT11b and TFT11c are ON states. Moreover, the Vgh electrical potential difference is impressed to gate signal line 17b (4). Therefore, the current is not flowing to EL element 15 of the pixel line which switching TFT11d of a pixel line (4) is an OFF state, and corresponds. That is, it is in the astigmatism LGT condition 312. The Vgl electrical potential difference is impressed to gate signal line 17b (3). Switching TFT11d is an ON state. Therefore, switching TFT11d of a pixel line (3) is an ON state, and EL element 15 of a corresponding pixel line emits light.

[0727] A write-in pixel line is eye (6) pixel lines the following 1H. The Vgl electrical potential difference is impressed to gate signal line 17a (6). Switching TFT11b and TFT11c are ON states. Moreover, the Vgh electrical potential difference is impressed to gate signal line 17b (6). Therefore, the current is not flowing to EL element 15 of the pixel line which switching TFT11d of a pixel line (6) is an OFF state, and corresponds. That is, it is in the astigmatism LGT condition 312. The Vgl electrical potential difference is impressed to gate signal line 17b (4). Switching TFT11d is an ON state. Therefore, switching TFT11d of a pixel line (4) is an ON state, and EL element 15 of a corresponding pixel line emits light.

[0728] As mentioned above, sequential selection of the even-pixel line is made, and image data is written and crowded with the 2nd field. The image display of one sheet is completed in this 1st field and 2nd field. Moreover, in the 2nd field, when writing an even-pixel line, all odd-pixel lines are taken as the astigmatism LGT display 312. In the 1st field, when writing an odd-pixel line, all even-pixel lines are taken as the astigmatism LGT display 312.

[0729] However, if a current (N= 10) is carried out the source signal line 18 10 times and a current program is carried out to a sink and TFT11a, even if it will carry out processing in which an odd-pixel line or an even-pixel line is displayed by turns, by the drive approach of drawing 154, display brightness turns into the one 2= 5 times brightness [10 /] of this of predetermined brightness. Therefore, in order to make display brightness into 1 time, it is necessary to drive by N= 2. However, if it drives by N= 2, the current value written in the source signal line 18 cannot fully carry out the charge and discharge of the parasitic

capacitance 404 small. Therefore, it writes in a capacitor 19, lack occurs, and resolution falls.
[0730] What is necessary is just to set an odd-pixel line or not only an even-pixel line but some of display screens 21 to astigmatism LGT field 312a so that it may illustrate to drawing 156 in order to solve with this. drawing 156 -- drawing -- it is scanned with 156(a) -> Fig. 156(b) -> Fig. 156(c) -> Fig. 156 (a). As shown in drawing 156 (b), a viewing area is formed in the write-in pixel line 871a bottom in the predetermined range (while scanning down from on a screen). However, since a viewing area is an odd-pixel line or an even-pixel line, it becomes for every 1-pixel line. Astigmatism LGT field 312a is made into the continuous astigmatism LGT field.
[0731] However, like the drive approach of drawing 156, if a viewing area is hardened and scanned to the display screen at a part, it will become easy to generate a flicker. However, when a frame rate is 80Hz or more, even if it is in the display condition of drawing 156 (when a viewing area 311 is set to one), cautions are taken for there to be no generating of a flicker. That is, if a frame rate is set to 80Hz or more, it is not necessary to divide the lighting field 311.
[0732] What is necessary is just to divide so that it may illustrate to drawing 157 when a frame rate is low. This was explained above. Therefore, probably, drawing 157 does not have **** in explanation daringly. However, drawing 157 was plotted in the pair of astigmatism LGT field 312b and the lighting field 311 as a divided field in order to make a plot easy. However, it cannot be overemphasized that two or more astigmatism LGT field 312b and two or more lighting fields 311 exist in the divided field instead of what is limited to this.
[0733] Various configurations can be considered to a drive method. In drawing 158, when a write-in pixel line is eye (1) pixel line, as for gate signal line 17a, (1) and (G) are chosen. That is, switching TFT11b of a pixel line (1) and (G) and TFT11c are ON states. Moreover, the Vgh electrical potential difference is impressed to gate signal line 17b. Therefore, the current is not flowing to EL element 15 of the pixel line which switching TFT11d of a pixel line (1) and (G) is an OFF state at least, and corresponds. That is, it is in the astigmatism LGT condition 312.
[0734] Since the pixel line chosen as coincidence is a 2-pixel line (K= 2), two drive TFT11a operates. That is, per pixel, and 10 / 2= 5 times as many current as this flows to TFT11a. In the source signal line 18, the current which added two program currents of TFT11a flows.
[0735] After the following 1H, gate signal line 17a (G) is un-choosing, and ON state voltage (Vgl) is impressed to gate signal line 17b. Moreover, gate signal line 17a (2) is chosen as coincidence (Vgl electrical potential difference), and a program current flows from TFT11a of the selected pixel line (2) to the source signal line 18 toward the source driver 14. Thus, from that of operating, the image data of normal is held at a pixel line (G).
[0736] After the following 1H, gate signal line 17a (1) is un-choosing, and ON state voltage (Vgl) is impressed to gate signal line 17b. Moreover, gate signal line 17a (3) is chosen as coincidence (Vgl electrical potential difference), and a program current flows from TFT11a of the selected pixel line (3) to the source signal line 18 toward the source driver 14. Thus, from that of operating, the image data of normal is held at a pixel line (1). one screen is rewritten by scanning, shifting a 1-pixel line every with the above actuation.
[0737] What is necessary is just to divide the astigmatism LGT field 312 or the lighting field 311 into plurality so that it may illustrate to drawing 160 when it is easy to generate a flicker. This was explained above. Therefore, probably, drawing 157 does not have **** in explanation daringly.
[0738] Drawing 161 is a false interlace drive. With a false interlace drive, the 1st F (the 1st field) chooses the 2-pixel (two or more pixels) line of an odd-pixel line and an even-pixel line as coincidence, and it writes in image data, without the selected pixel line lapping. The 2nd following F is a method which writes in image data, without the pixel line which chose and

chose the 2-pixel (two or more pixels) line of an even-pixel line and an odd-pixel line as coincidence lapping except for the 1st pixel line.

[0739] Drawing 161 (a1) (a2) (a3) is the 1st field, and drawing 161 (b1) (b2) (b3) is the 2nd field. The 1st field writes in image data for drawing 161 (a1) -> drawing 161 (a2) -> drawing 161 (a3) -> and the sequential write-in pixel line 871 in a 2-pixel line pair. Therefore, a 2-pixel line is the same image display, and period maintenance of the 1 field is carried out for this display condition. Moreover, in the 1st field, the image data of an odd-pixel line is displayed on the odd pixel line of relevance, and the following even-pixel line. That is, the image data of the 1st line is displayed on the 1st pixel line and the 2nd pixel line, the image data of the 3rd line is displayed on the 3rd pixel line and the 4th pixel line, the image data of the 5th line is displayed on the 5th pixel line and the 6th pixel line, and the image data of the 7th line is displayed on the 7th pixel line and the 8th pixel line. Hereafter, it is the same.

[0740] The 2nd field writes in image data for drawing 161 (b1) -> drawing 161 (b2) -> drawing 161 (b3) -> and the sequential write-in pixel line 871 in a 2-pixel line pair. Therefore, a 2-pixel line is the same image display, and period maintenance of the 1 field is carried out for this display condition. Moreover, in the 2nd IRUDO, the image data of an even-pixel line is displayed on the even pixel line of relevance, and the following odd-pixel line. That is, the image data of the 2nd line is displayed on the 2nd pixel line and the 3rd pixel line, the image data of the 4th line is displayed on the 4th pixel line and the 5th pixel line, the image data of the 6th line is displayed on the 6th pixel line and the 7th pixel line, and the image data of the 8th line is displayed on the 8th pixel line and the 9th pixel line. Hereafter, it is the same.

[0741] In addition, as for the 1st pixel line of drawing 161 (a1), the condition of the 1st field is kept held. Moreover, reverse is sufficient, although [in the 1st field] odd number image data is written in and even number image data is written in in the 2nd field. That is, though even number image data is written in and odd number image data is written in in the 2nd field, it is good in the 1st field.

[0742] When carrying out image display as mentioned above, and when human being's eyes add the display image of the 2 fields by the after-image, and can be put together and seen and one frame (2 field) is completed, the 1st pixel line is the display image of the 1st field. Moreover, as for the 2nd pixel line, the image data of the 1st pixel line of the 1st field and the image data of the 2nd pixel line of the 2nd field were added. As for the 3rd pixel line, the image data of the 3rd pixel line of the 1st field and the image data of the 2nd pixel line of the 2nd field were added. Moreover, as for the 4th pixel line, the image data of the 3rd pixel line of the 1st field and the image data of the 4th pixel line of the 2nd field were added. As for the 5th pixel line, the image data of the 5th pixel line of the 1st field and the image data of the 4th pixel line of the 2nd field were added. Hereafter, it is the same.

[0743] As mentioned above, since each pixel line becomes that to which the image of the two fields piled up and was joined, the profile of a display image becomes smooth. Although some animation dotage especially occurs in a movie display, good resolution is mostly obtained with a still picture (recognized like).

[0744] Drawing 162 is a drive wave for realizing the method of presentation of drawing 161. The upper location of a drawing is the drive wave of the 1st field (1F), and the inferior surface of tongue of a drawing is the drive wave of the 2nd field (2F).

[0745] In the 1st field (1F), gate signal line 17of 1st pixel line and 2nd pixel line a (1) and (2) are chosen first. To the source signal line 18, a 10 times (N= 10) as many drive current as this flows. Therefore, it is programmed by drive TFT11a of a pixel line (1) and (2) with a 5 times as many current as this, respectively. At this time, a Vgh electrical potential difference is impressed to gate signal line 17of 1st pixel line and 2nd pixel line b (1), and (2), and TFT11d is an OFF state. Therefore, EL element 15 of the 1st pixel line and the 2nd pixel line is not turned on.

[0746] gate signal line 17of 3rd pixel line and 4th pixel line a (3) and (4) are chosen after 2H (since even-pixel line or odd-pixel line [every] image data is written in, set to 2H). To the source signal line 18, a 10 times (N= 10) as many drive current as this flows. Therefore, it is programmed by drive TFT11a of a pixel line (3) and (4) with a 5 times as many current as this, respectively. At this time, a Vgh electrical potential difference is impressed to gate signal line 17of 3rd pixel line and 4th pixel line b (3), and (4), and TFT11d is an OFF state. Therefore, EL element 15 of the 3rd pixel line and the 4th pixel line is not turned on.

[0747] On the other hand, a Vgl electrical potential difference is impressed to gate signal line 17b (1) and (2). Therefore, TFT11d of the 1st pixel line and the 2nd pixel line is turned on, and EL element 15 is turned on.

[0748] Furthermore, gate signal line 17of 5th pixel line and 6th pixel line a (5) and (6) are chosen after 2H. To the source signal line 18, a 10 times (N= 10) as many drive current as this flows. Therefore, it is programmed by drive TFT11a of a pixel line (5) and (6) with a 5 times as many current as this, respectively. At this time, a Vgh electrical potential difference is impressed to gate signal line 17of 5th pixel line and 6th pixel line b (5), and (6), and TFT11d is an OFF state. Therefore, EL element 15 of the 5th pixel line and the 6th pixel line is not turned on.

[0749] On the other hand, a Vgl electrical potential difference is impressed to gate signal line 17b (1), (2), (3), and (4). Therefore, TFT11d of the 1st pixel line, the 2nd pixel line, the 3rd pixel line, and the 4th pixel line is turned on, and EL element 15 is turned on. The above actuation is carried out to the odd pixel line of last of a screen, and one screen is displayed.

[0750] The 1st pixel line does not choose but makes the condition of the 1st field hold in the 2nd field (2F). Next, gate signal line 17of 2nd pixel line and 3rd pixel line a (2) and (3) are chosen. To the source signal line 18, a 10 times (N= 10) as many drive current as this flows. Therefore, it is programmed by drive TFT11a of a pixel line (2) and (3) with a 5 times as many current as this, respectively. At this time, a Vgh electrical potential difference is impressed to gate signal line 17of 2nd pixel line and 3rd pixel line b (2), and (3), and TFT11d is an OFF state. Therefore, EL element 15 of the 2nd pixel line and the 3rd pixel line is not turned on.

[0751] Gate signal line 17of 4th pixel line and 5th pixel line a (4) and (5) are chosen after 2H. To the source signal line 18, a 10 times (N= 10) as many drive current as this flows. Therefore, it is programmed by drive TFT11a of a pixel line (4) and (5) with a 5 times as many current as this, respectively. At this time, a Vgh electrical potential difference is impressed to gate signal line 17of 4th pixel line and 5th pixel line b (4), and (5), and TFT11d is an OFF state. Therefore, EL element 15 of the 4th pixel line and the 5th pixel line is not turned on.

[0752] On the other hand, a Vgl electrical potential difference is impressed to gate signal line 17b (2) and (3). Therefore, TFT11d of the 1st pixel line, the 2nd pixel line, and the 3rd pixel line is turned on, and EL element 15 is turned on.

[0753] Furthermore, gate signal line 17of 6th pixel line and 7th pixel line a (6) and (7) are chosen after 2H. To the source signal line 18, a 10 times (N= 10) as many drive current as this flows. Therefore, it is programmed by drive TFT11a of a pixel line (6) and (7) with a 5 times as many current as this, respectively. At this time, a Vgh electrical potential difference is impressed to gate signal line 17of 6th pixel line and 7th pixel line b (6), and (7), and TFT11d is an OFF state. Therefore, EL element 15 of the 6th pixel line and the 7th pixel line is not turned on.

[0754] On the other hand, a Vgl electrical potential difference is impressed to gate signal line 17b (1), (2), (3), (4), and (5). Therefore, TFT11d of the 1st pixel line, the 2nd pixel line, the 3rd pixel line, the 4th pixel line, and the 5th pixel line is turned on, and EL element 15 is turned on. The above actuation is carried out to the even pixel line of last of a screen, and one

screen is displayed.

[0755] The above example was what displays one screen in the 2 field. Drawing 163 displays one screen in the 2 or more fields. For drawing 163 (a), the 1st field and drawing 163 (b) are [the 2nd field and drawing 163 (c)] the 3rd field.

[0756] In the 1st field, a 4Y-3 (Y is one or more integers) pixel line and 4 Y-2-pixel line write in, and it is the pixel line 871. 2-pixel line [every] image data is written in. In the 2nd field, 4 Y-1-pixel line and 4 Y pixel line write in, and it is the pixel line 871. 2-pixel line [every] image data is similarly written in for the previous field. In the 3rd field, 4 Y-2-pixel line and 4 Y-1-pixel line write in, and it is the pixel line 871. 2-pixel line [every] image data is written in. Each pixel data is interpolated by the image data of two or more fields from that of writing in by 3F as mentioned above.

[0757] Although drawing 163 was the example of one screen in the 3 fields, image display may be realized using the field beyond it. For example, in the case of the 4 field, a 4Y-3 (Y is one or more integers) pixel line and 4 Y-2-pixel line write in, and it is the pixel line 871 in the 1st field. 2-pixel line [every] image data is written in. In the 2nd field, 4 Y-1-pixel line and 4 Y pixel line write in, and it is the pixel line 871. In the 3rd field, 4 Y-2-pixel line and 4 Y-1-pixel line write in, and it is the pixel line 871. 2-pixel line [every] image data is written in like the point. In the 4th field, 4 Y-3-pixel line and 4 Y pixel line write in, and it is the pixel line 871. 2-pixel line [every] image data is similarly written in for the previous field. Each pixel data is interpolated by the image data of two or more fields from that of writing in as mentioned above in the 4 fields.

[0758] Although the above example mainly illustrated and explained the pixel configuration of drawing 1, its drive method of this invention is effective also to other current program pixel configurations, such as drawing 21, drawing 43, drawing 71, and drawing 76.

[0759] Drawing 164 is an explanatory view of the drive approach of the pixel configuration of drawing 76. In addition, in order to give explanation easy, the current (or the current which the source driver IC 14 absorbs from the source signal line 18, the current which drive TFT11a slushes into the source signal line 18) passed from the source driver IC 14 to the source signal line 18 explains as 10 times (N= 10) of a predetermined value also here. Moreover, the current scale factor of TFT11a and TFT11b explains noting that it is 1:1 (current scale factor 1).

[0760] Therefore, if the pixel line chosen as coincidence is a 5-pixel line (K= 5), five drive TFT11a will operate. Since it is the current scale factor 1, the same current as TFT11a flows also to TFT11b. That is, per pixel, and 10 / 5= 2 twice as many current as this flows to TFT11a. Since the current programmed by TFT11a of a pixel 16 is twice the predetermined value, the current which flows to EL is also twice. Therefore, degradation of EL element 15 decreases as compared with the case where a 10 times as many current as this is passed like drawing 87. Since the current which flows to the source signal line 18 on the other hand is 10 times, the charge and discharge of the same parasitic capacitance 404 as drawing 87 are possible for it. This is the same also in drawing 88.

[0761] If a current scale factor is 2, the current which TFT11b passes to EL element 15 will become 1 time. Therefore, the predetermined current which can obtain predetermined brightness can be passed to EL element 15. That is, the drive design of a high display panel whenever general-purpose is possible by designing a current scale factor (rate of a current ratio of TFT11a and TFT11b), and the current (program current) passed to the source signal line 18 with the pixel configuration of drawing 21, drawing 43, drawing 71, and drawing 76 (adjustment).

[0762] If the pixel line chosen as coincidence is a 5-pixel line (K= 5), it will become what added five program currents of TFT11a. For example, originally, it considers as the current Id to write in and the current of Idx10 is passed to N= 10, then the source signal line 18 at write-

in pixel line 871a. Pixel line 871b which adjoined write-in pixel line 871a (871b is a pixel line used auxiliary in order to make the amount of currents to the source signal line 18 increase.) Therefore, the pixel (line) which writes in an image is 871a, and in order to write in 871a, 871b uses [a pixel (line)] auxiliary.

[0763] In drawing 164, it writes in K line (K= 5) coincidence by the image data of write-in pixel (line) 871a. Therefore, the range of K lines (871a, 871b) serves as the same display. Thus, if it is made the same display, resolution will fall with a natural thing. In order to cope with this, it writes in so that it may illustrate to drawing 88 (b), and the part of pixel line 871b is considered as the astigmatism LGT display 312. Therefore, a resolution fall is not generated.

[0764] Since this pixel is under program, although 871a illustrated to drawing 164 (a) is changed into the display condition, it changes in the state of the current writing to a pixel. Therefore, it is good also as a non-display field 312.

[0765] After the following 1H writes in the pixel line which carried out the 1-pixel line shift, and performs the same actuation as pixel line 871a. The 1-pixel (line) shift also of the astigmatism LGT field 312 is carried out. As mentioned above, 871b in which different current data from an original indicative data were written is not displayed. If it shifts the above actuation of one line at a time, perfect image display is realizable. Moreover, the charge and discharge of parasitic capacitance 404 are also realizable within 1H period enough by the effectiveness of pixel line 871b used auxiliary.

[0766] Drawing 165 is an explanatory view of a drive wave for realizing the drive approach of drawing 164. A voltage waveform sets OFF state voltage to Vgh (H level), and is setting ON state voltage to Vgl (L level). Moreover, the number of the pixel line chosen as the lower berth of drawing 165 is indicated. Moreover, (1), (2), (3) ... (11) shows the chosen pixel line number. Therefore, a pixel line count is 480 by the VGA panel, and is 768 by the XGA panel.

[0767] In drawing 165, gate signal line 17a (1) and gate signal line 17b (1) are chosen (Vgl electrical potential difference), and a program current flows from TFT11a of the selected pixel line to the source signal line 18 toward the source driver 14. Moreover, the program current which flows to the source signal line 18 is N times (in order to give explanation easy, it explains as N= 10.) of a predetermined value. of course, since a predetermined value is a data current which displays an image, unless it is white raster display etc., it is not a fixed value. it is . Moreover, a 5-pixel line explains to coincidence as selection (K= 5). Therefore, ideally, it is programmed by the capacitor 19 of one pixel so that a current flows twice at TFT11a.

[0768] Fundamentally, since the gate signal lines 17a and 17b are the same phases, communalizing is possible. However, strictly in case choosing a pixel line and un-choosing, it is desirable to control so that TFT11d turns off and then TFT11c turns off first. Therefore, as for gate signal line 17a and gate signal line 17b, dissociating is desirable.

[0769] When a write-in pixel line is eye (1) pixel line, as illustrated in drawing 164, the Vgl electrical potential difference is impressed to the gate signal lines 17a and 17b. Therefore, a pixel line (1), (2), (3), (4), and (5) are chosen. That is, switching TFT11c of a pixel line (1), (2), (3), (4), and (5) and TFT11d are ON states. Moreover, gate signal line 17b is the opposite phase of gate signal line 17b. Therefore, the current is not flowing to EL element 15 of the pixel line which switching TFT11d of a pixel line (2), (3), (4), and (5) is an OFF state, and corresponds. That is, it is in the astigmatism LGT condition 312.

[0770] Ideally, 5-pixel TFT11a passes the current of Idx2 to the source signal line 18, respectively. And a twice as many current as this is programmed by the capacitor 19 of each pixel 16. Here, in order to make an understanding easy, it explains noting that the property (Vt, S value) of each TFT11a corresponds.

[0771] Since the pixel line chosen as coincidence is a 5-pixel line (K= 5), five drive TFT11a

operates. That is, per pixel, and 10 / 5= 2 twice as many current as this flows to TFT11a. In the source signal line 18, the current which added five program currents of TFT11a flows. For example, originally, it considers as the current Id to write in and the current of Idx10 is passed to the source signal line 18 at write-in pixel line 871a.

[0772] Four write-in pixel line 871b which writes in image data henceforth from a write-in pixel line (1) is a pixel line used auxiliary in order to make the amount of currents to the source signal line 18 increase. However, since the image data of normal is written in behind, write-in pixel line 871b is satisfactory.

[0773] Therefore, pixel line 871b is the same display as 871a between 1H periods. Therefore, pixel line 871b chosen in order to make a current increase is made into the non-display condition 312 at least.

[0774] After the following 1H, gate signal line 17a (1) and 17b (1) are un-choosing (location of the pixel line number 6), and the data written in a pixel decide them. Moreover, gate signal line 17a (6) is chosen as coincidence (location of the pixel number 2), and a program current flows from TFT11a of the selected pixel line (6) to the source signal line 18 toward the source driver 14. Thus, from that of operating, the image data of normal is held at a pixel line (1).

[0775] After the following 1H, gate signal line 17a (2) and 17b (2) are un-choosing. Moreover, gate signal line 17a (7) is chosen (Vgl electrical potential difference), and a program current flows from TFT11a of the selected pixel line (7) to the source signal line 18 toward the source driver 14. Thus, from that of operating, the image data of normal is held at a pixel line (2). one screen is rewritten by scanning, shifting a 1-pixel line every with the above actuation.

[0776] Although it is the same as that of drawing 134, in order to program with a twice as many current (electrical potential difference) as this to each pixel, by the drive approach of drawing 140, the luminescence brightness of EL element 15 of each pixel becomes twice ideally. Therefore, the brightness of the display screen becomes twice from a predetermined value.

[0777] What is necessary is just to let one half of the range of a viewing area 21 be the non-display fields 312, including the write-in pixel line 871 so that you may illustrate to drawing 87 in order to make this into predetermined brightness. Since this was explained using drawing 137 etc., it omits explanation. In addition, it cannot be overemphasized that the drive method of drawing 146 is also applicable to drawing 43, drawing 71, drawing 164, drawing 76, drawing 54, drawing 67, drawing 68, drawing 103, etc. Since it is carrying out before, explanation is omitted.

[0778] The animation display engine performance improves, so that area of the black viewing area (non-display field) 312 occupied to the display screen 21 is enlarged. Therefore, what is necessary is to lessen the non-display field 311 so that it may illustrate to drawing 141, and just to enlarge area of the non-display field 312.

[0779] In the example of this invention, a program current (electrical potential difference) can be adjusted by changing the current (electrical potential difference) passed to the source signal line 18. That is, the current which flows to the source signal line 18 can be adjusted only by adjusting the reference current (electrical potential difference) of the source driver 14. It can be set up by the data to ST* terminal impressed to the shift register 22 of the gate driver 12 illustrated to drawing 2 etc. whether coincidence is made whether coincidence is made to turn on a 2-pixel line or to turn on a 5-pixel line or only a 1-pixel line is chosen. Therefore, the specification of the source driver 14 is not influenced by the number of pixels to choose.

[0780] Moreover, since the brightness of a screen can also be adjusted by turning on and off of gate signal line 17c, the output current from the source driver 14 is not changed by

brightness adjustment of Screen 21. Therefore, what is necessary is just to determine the gamma property of EL element 15 to one current. Therefore, the configuration of the source driver 14 is very easy, and becomes the high thing of versatility. It cannot be overemphasized that the above matter is applicable also to the example of other this inventions.

[0781] If a frame rate is low like drawing 136 when one viewing area 311 moves to down from on a screen, as shown in drawing 164, it will be recognized visually that a viewing area 311 moves. It becomes that it is easy to be recognized when a palpebra is closed especially, or when moving a face up and down. It is good to divide a viewing area 311 into plurality so that it may illustrate to drawing 142 to this technical problem.

[0782] In addition, the scanning direction of the astigmatism LGT viewing area 312 is not limited only to down from on a screen so that it may illustrate to drawing 142 (b). You may scan above from under a screen. moreover, the scanning direction from a top to the bottom and the scanning direction from the bottom to above -- alternation -- or you may scan at random. Moreover, it cannot be overemphasized that the number of partitions may be changed in the predetermined location of every frame and the display screen 21.

[0783] As mentioned above, a flicker of a screen decreases by dividing a viewing area 311 into plurality. Therefore, there is no generating of a flicker and it can realize good image display. In addition, division may be made finer. However, the more it divides, the more a flicker is mitigated. Since especially the responsibility of EL element 15 is quick, even if it turns on and off by time amount smaller than 5microsec, there is no fall of display brightness.

[0784] Although drawing 87 and drawing 88 illustrated and explained the pixel configuration of drawing 1, drawing 76, drawing 21, drawing 43, and a current program method like drawing 71, they are not limited to this. For example, the pixel configuration of electrical-potential-difference program methods, such as drawing 54, drawing 68, and drawing 103, is also effective. Since a pixel can be ******(ed) by considering as the method which impresses an electrical potential difference at coincidence at two or more pixel line, it can respond also to the highly minute display panel more than SXGA. Moreover, it is because a ****** circuit and a digital disposal circuit are simplified and a good black display can be realized.

[0785] It explains by illustrating the pixel configuration of drawing 54 as an example of application of an electrical-potential-difference program. In addition, drawing 166 and drawing 167 are the drive wave. Although it explains noting that a 5-pixel line is made into the astigmatism LGT field 312 in drawing 166 and drawing 167, it does not limit to this. It is for only giving explanation easy. For example, coincidence selection of the 2-pixel line may be made, and a 10-pixel line is sufficient. Moreover, it is good also considering a 1-pixel line as an astigmatism LGT field 312. This is the same also to drawing 54, drawing 67, drawing 68, drawing 103, etc.

[0786] Moreover, it cannot be overemphasized that the drive method explained in drawing 144, drawing 146, drawing 151, drawing 152, drawing 154, drawing 163, etc. is applicable to the pixel configuration of the electrical-potential-difference program illustrated in drawing 54, drawing 67, drawing 68, drawing 103, etc. Moreover, it cannot be overemphasized that the drive method of driving so that a N times as many current as this may flow to EL element 15, and forming the astigmatism LGT field 312 is also applicable. However, since explanation becomes complicated, drawing 166 and drawing 167 do not dare explain.

[0787] It writes in, as shown in drawing 167, and when a pixel line is eye (1) pixel line, as for gate signal line 17a, (1), (2), (3), (4), and (5) are chosen (location of the pixel line number 5). That is, switching TFT11b of a pixel line (1), (2), (3), (4), and (5) is an ON state. OFF state voltage (Vgh) is impressed to gate signal line 17b. Therefore, the current is not flowing to EL element 15 of the pixel line which switching TFT11d of a pixel line (1), (2), (3), (4), and (5) is an OFF state, and corresponds. That is, it is in the astigmatism LGT condition 312. Therefore, preliminary charge of the period of 5H and the electrical potential difference will

be carried out at the pixel line (1).

[0788] The pixel line by which preliminary charge is carried out is the display same between 5H periods as other 4-pixel lines. Therefore, the pixel line which is writing in is made into the non-display condition 312 at least. Image data approximate especially in the pixel which adjoined in the video signal. Therefore, if preliminary charge is performed, the writing of the image data of normal will become easy.

[0789] Therefore, this invention is the approach of making it into the non-display condition 312 until it writes image data in two or more pixel lines and the image data of normal is written in. However, since the display is unstable while writing in the image data of this pixel line even if it is selection of a 1-pixel line, it is also the concept of this invention to suppose that it is non-display. Moreover, the current which flows to EL element 15 is made larger than a predetermined value, and it is made predetermined brightness by forming the astigmatism LGT field 312. The effectiveness of this invention also realizes a good animation with this method of presentation.

[0790] The image data of eye (2) pixel lines is made to decide in the following 1H. OFF state voltage is impressed to gate signal line 17a (1) and gate signal line 17b (1) so that clearly [in drawing 167] (pixel line number 6). (since Vgl:TFT11b is n channels) ON is impressed to gate signal line 17a (6) and gate signal line 17b (6) (since Vgh:TFT11b is n channels). Therefore, the image data to TFT11a of a pixel line (2) is held.

[0791] Synchronizing with a horizontal scanning period, a 1-pixel line and a write-in pixel line shift as mentioned above. One screen can be displayed by carrying out the above actuation one by one.

[0792] Drawing 166 is the shifted method 1H about the timing of gate signal line 17b in the pixel configuration of drawing 54. The pixel to decide is made into a display condition although it is clear in drawing 166.

[0793] For example, as for the pixel line (1), the period of 5H and image data are written in (period of the pixel line number 1-5). That is, gate signal line 17a of a pixel line (1) is in a selection condition (since TFT11b is n channels, Vgh is impressed). Since ON state voltage is impressed to gate signal line 17b (1) at the time of 5H (since Vgl:TFT11d is P channels), the current is flowing to EL element 15. Therefore, EL element 15 is in a lighting condition. This point differs from drawing 167. In drawing 167, it was considering as the astigmatism LGT field 312. Since other points are the same as that of drawing 167, explanation is omitted.

[0794] in addition, the example of this invention which coincidence is made to turn on two or more above pixel lines, and writes in image data -- setting -- the maximum surface or the lowest side of a viewing area 21 -- or the pixel line of the both does not have the adjoining pixel line which coincidence is made to turn on. this technical problem -- receiving -- the maximum surface or the lowest side of a viewing area 21 -- or what is necessary is just to form or arrange a dummy pixel line to those both

[0795] For example, by the drive method which chooses as coincidence the 5-pixel line explained in drawing 139, four pixel lines are formed the lower side of a screen. When carrying out a vertical reversal drive, of course, four dummy pixel lines are prepared also in the surface of a screen. A dummy pixel line does not form EL element 15. Therefore, luminescence is not carried out. Even if it forms EL element 15, of course, it is made not to emit light, or it shades and is made not to be displayed. In addition, in drawing 1, you may form except 1-pixel TFT11d. A dummy pixel line is formed more than a 1-pixel line.

[0796] Moreover, although carried out to making coincidence turn on the adjoining pixel line, it does not limit to this. For example, the timing which makes two or more pixel lines turn on may differ. Moreover, the effectiveness is demonstrated even if separated from the 1st line like the 2-pixel line of the 3rd line. Extremely, when choosing a 2-pixel line, a 1-pixel line is made to fix and turn on (for example, the bottom pixel line or bottom dummy pixel line of a

screen), other 1-pixel lines may be scanned and sequential ON may be carried out.

[0797] TFT for a drive to which the above example passes a current to EL element 15 fundamentally was what the number of is one and displays target brightness on 1 pixel in the 1 field (one frame). However, this invention is not limited to this. Hereafter, the example is explained.

[0798] Drawing 309 is based on the pixel configuration of the current program of drawing 1. The difference between drawing 1 and drawing 309 is the point that drawing 309 is formed in one pixel in TFT 11a1 and two of TFT11a2 as TFT for a drive (production). Moreover, switching TFT1f1 which turns on and off the current path of TFT 11a1 and EL element 15 (cutting, connection) is formed (arrangement). Furthermore, switching TFT1f2 which turns on and off the current path of TFT 11a2 and EL element 15 (cutting, connection) is formed (arrangement). 1 is connected to the gate (G) terminal of this TFT11f1 17f of gate signal lines, and TFT11f1 turns on by impressing a Vgh electrical potential difference to 1 17f of this gate signal line (TFT11f1 turns off by impressing a Vgl electrical potential difference). Similarly, 2 is connected to the gate (G) terminal of this TFT11f2 17f of gate signal lines, and TFT11f2 turns on by impressing a Vgh electrical potential difference to 2 17f of this gate signal line (TFT11f2 turns off by impressing a Vgl electrical potential difference). Of course, each gate signal line 17 is common to a pixel line. Identically to the actuation explained by drawing 1, or similar, since other actuation etc. is [that a configuration is also the same or] similar, it omits explanation.

[0799] Drawing 310 and drawing 311 are [the following and] explanatory views of actuation of the pixel configuration of drawing 309. In drawing 310 and drawing 311, the notation of a switch is illustrating switching TFT11.

[0800] Let the current which flows to EL element 15 be a predetermined value by two frames (2 field) with the configuration of drawing 309. Here, in order to give explanation easy, it explains noting that the current which flows to EL element 15 in the period of two frames is made into a predetermined value. Moreover, the current to program is set to Iw=10 (muA) (in addition, this is a temporary setup.). The current according to images, such as 1.2 (muA), shall be programmed actually, and the current according to the programmed current Iw shall flow to EL element 15.

[0801] Fundamentally, it is the 1st frame and program current Iw=10 (muA) is absorbed to the source driver 14. This current Iw is supplied to a pixel from both two drives TFT. In the 1st frame, 1st drive TFT11a is chosen and this current is passed to EL element 15. EL element 15 emits light according to the current of this 1st drive TFT11a. Program current Iw=10 [frame / 2nd / at least] (muA) is absorbed to the source driver 14 like the 1st frame. This current Iw is supplied to a pixel from both two drives TFT.

[0802] In the 2nd frame, 2nd drive TFT11a is chosen and this current is passed to EL element 15. EL element 15 emits light according to the current of this 2nd drive TFT11a. Therefore, if a two-frame period is averaged, EL element 15 will emit light by the brightness according to the average current which 1st drive TFT11a and 2nd drive TFT11a pass. If it is program current Iw=10 (muA), light will be emitted by the brightness of 10 / 2= 5 (muA). Therefore, even if the property of two drives TFT11 has shifted, the same program current Iw is passed and the current program of two drives TFT is carried out. And the current correctly programmed in the two-frame period in these two drives TFT since the current was passed to EL element 15 by a unit of 1 time in the two-frame period can be passed to an EL element.

[0803] In addition, it was not based on the drive TFT property variation of a pixel by two frames, but the above explanation explained for obtaining target brightness. However, when displaying the image of an animation etc., this need does not exist. What is necessary is just to only pass two drive TFT11a to EL element 15 by turns mechanically. It is this example that the sum of the current correctly passed to EL element 15 in the two-frame period is in

agreement with a program current. However, by the animation, the image is changing continuously. Therefore, it is because it is not visually recognized by the animation even if a display condition shifts. in addition, in a still picture, since there is no motion of an image, it sees to image display and who does not come out Hereafter, it explains to a detail further.

[0804] Drawing 310 is in the condition that an applicable pixel is chosen and the current program is performed. ON state voltage (Vgl) is impressed to gate signal line 17a, and TFT11b and TFT11c turn on. The program current Iw flows toward the source driver (not shown) 14 from TFT1a. At this time, TFT11d is an OFF state (OFF state voltage (Vgh) is impressed to gate signal line 17b). ON state voltage (Vgl) is impressed also to 2 17f 1 and 17f of gate signal lines of gate signal lines, and TFT11f1 and TFT11f2 are ON states.

[0805] The program current Iw is supplied from TFT 11a1 for a drive, and TFT11a2. When the current to which Ia1 and TFT 11a2 supply the current which TFT 11a1 supplies is set to Ia2, it is program current Iw=Ia1+Ia2.

[0806] Originally, since TFT 11a1 and TFT11a2 adjoin and they are formed, they should not almost have a property gap. however -- case it formed with the low-temperature polish recon technique -- **** -- Vt electrical potential differences etc. differ. Therefore, drive TFT 11a1 and the gate terminal of TFT11a2 are carried out in common, and even if it impresses the same electrical potential difference to this gate terminal, drive TFT 11a1 differs from the current which TFT11a2 pass. In things, in order to give explanation easy, they explain noting that TFT 11a1 and TFT11a2 have the difference of 3:7. That is, if program current Iw=10 (muA), TFT 11a1 will supply the current of 3 (muA), and TFT 11a2 will presuppose it that the current of 7 (muA) is supplied. That is, it is program current Iw=Ia1+Ia2=3(muA)+7(muA) =10 (muA).

[0807] If a pixel will be in the condition of not choosing, it will be in the condition of drawing 311 (a). OFF state voltage (Vgh) is impressed to gate signal line 17a, and TFT11b and TFT11c turn off. ON state voltage (Vgh) is impressed to gate signal line 17b at coincidence, and TFT11d turns on. ON state voltage (Vgl) is impressed to 1 17f of gate signal lines, and TFT11f1 turns on. Moreover, OFF state voltage (Vgh) is impressed to 2 17f of gate signal lines, and TFT11f2 is an OFF state.

[0808] Therefore, the current Idd1 from drive TFT 11a1 flows to EL element 15. If this current has TFT 11a1 and the same property of TFT11a2, it is Idd1=Iw / 2= 5 (muA). However, TFT 11a1 and the property of TFT11a2 are shifted actually. Here, in order to give explanation easy, it explains as Idd 1= 3 (muA) of TFT 11a1. Therefore, at the 1st frame, EL element 15 emits light with the current of 3 (muA).

[0809] In the 2nd frame next to the 1st frame, actuation explained in drawing 310 is performed again. That is, it is in the condition that an applicable pixel is chosen and the current program is performed. Like the 1st frame, ON state voltage (Vgl) is impressed to gate signal line 17a, and TFT11b and TFT11c turn on. Program current Iw=10 (muA) flows toward the source driver (not shown) 14 from TFT1a. ON state voltage (Vgl) is impressed also to 2 17f 1 and 17f of gate signal lines of gate signal lines, and TFT11f1 and TFT11f2 are ON states. Moreover, it is supplied from TFT 11a1 for a drive, and TFT11a2 like [current / Iw / program] the 1st frame.

[0810] If a pixel will be in the condition of not choosing, in the 2nd frame, it will be in the condition of drawing 311 (b). OFF state voltage (Vgh) is impressed to gate signal line 17a, and TFT11b and TFT11c turn off. ON state voltage (Vgh) is impressed to gate signal line 17b at coincidence, and TFT11d turns on. OFF state voltage (Vgh) is impressed to 1 17f of gate signal lines, and TFT11f1 turns off. Moreover, 17f of gate signal lines, ON state voltage (Vgl) is impressed to 2, and TFT11f2 is turned on in it.

[0811] Therefore, the current Idd2 from drive TFT 11a2 flows to EL element 15 shortly. If this current had TFT 11a1 and the same property of TFT11a2, the 1st-frame explanation

explained the point that it was Idd1=Iw / 2= 5 (muA). However, TFT 11a1 and the property of TFT11a2 are shifted actually. Here, in order to give explanation easy, it explains as Idd 2= 7 (muA) of TFT 11a2. Therefore, at the 2nd frame, EL element 15 emits light with the current of 7 (muA).

[0812] Illustration **** will be in the condition of drawing 312 in the state of a display about the above condition. The number of drawings 312 (a) is the 1st, and drawing 312 (b) is in the condition of the 2nd frame. That is, in the 1st frame, it writes in, the pixel line 871 is chosen and the current of 10 (muA) flows to the source signal line 18. And a current program is carried out at a pixel 16, and the current of 3 (muA) is passed by EL element 15 by TFT 11a1.

[0813] In the 2nd frame, it writes in, the pixel line 871 is chosen and the current of 10 (muA) flows to the source signal line 18 so that it may illustrate to drawing 312 (b). And a current program is carried out at a pixel 16, and the current of 7 (muA) is passed by EL element 15 by TFT 11a2. Therefore, if two frames is averaged, it will be set to (3 (muA)+7 (muA)) / 2= 5 (muA), and one half of the currents of program current Iw=10 (muA) will flow to EL element 15.

[0814] According to the above drive approach, even if two variations of the property of TFT11a for a drive formed in the pixel have occurred, variation is not generated on the average current which flows to EL element 15. That is, the current correctly proportional to the program current Iw (or the same) flows to EL element 15. Therefore, homogeneity image display is realizable.

[0815] In addition, in the above explanation, explain noting that you change TFT11a2 to TFT 11a1 for a drive which supplies a current to EL element 15 for every frame and a two-frame period carries out a current program with the same current at a pixel. However, when displaying the image of an animation etc., this need does not exist. The program current impressed to the source signal line 18 is changed for every frame according to a pixel, changes two drives TFT 11a1 and TFT11a2, and should just pass them to EL element 15 by turns. By the animation, the image is changing continuously. Therefore, it is because it is not visually recognized by the animation even if a display condition shifts. In addition, in a still picture, since there is no motion of an image, the current which flows to the source signal line 18 does not change for every frame. That is, in at least two frames, it is fixed.

[0816] In addition, also in the above case, to the source signal line 18, the twice (of course, it is twice [which averaged two frames] the current) of the current actually passed to EL are passed. Therefore, it writes in, even if parasitic capacitance 404 exists in the source signal line 18, and lack is mitigated. Moreover, the example of drawing 309 etc. is the technical thought of passing one half of the currents of the current passed to the source signal line 18 to EL element 15. This technical thought is the same as that of the method of passing a N times as many current as this to the source signal line 18, and passing the current of a sink and 1-/N to EL element 15 explained by drawing 87, drawing 88, etc.

[0817] In addition, TFT for a drive formed in 1 pixel is not limited to two pieces, as shown in drawing 309. Three or more pieces are sufficient. However, in order to control these TFT(s), the gate signal line 17 is needed in the switching TFT which turns the current of each TFT11a on and off (cutting, connection). Of course, said gate signal line 17 is common to a 1-pixel line. It cannot be overemphasized that the above matter is applied also in the following example or other examples.

[0818] The above example was the case of the pixel configuration of drawing 1. The technical thought which explained previously is applied also in the pixel configuration of drawing 21, drawing 43, drawing 71, and drawing 22. Drawing 313 is the example.

[0819] Actuation is the same as that of drawing 308. By the 1st frame, program current Iw=10 (muA) is absorbed to the source driver 14. This current Iw is supplied from drive TFT11a. In the 1st frame, the 1st drive TFT 11b1 is chosen, and this current is passed to EL

element 15. EL element 15 emits light according to the current of this 1st drive TFT 11b1.

[0820] Program current Iw=10 [frame / 2nd / at least] (muA) is absorbed to the source driver 14 like the 1st frame. In the 2nd frame, the 2nd drive TFT 11b2 is chosen, and this current is passed to EL element 15. EL element 15 emits light according to the current of this 2nd drive TFT 11b2. Therefore, if a two-frame period is averaged, EL element 15 will emit light by the brightness according to the average current which the 1st drive TFT 11b1 and the drive TFT of the 2nd 11b2 pass. If it is program current Iw=10 (muA), light will be emitted by the brightness of 10 / 2= 5 (muA). Therefore, even if two drives TFT 11b1 and the property of TFT11b2 have shifted, the same program current Iw is passed, the relation of a current mirror is maintained, and the current program of the TFT is carried out. And the current correctly programmed in the two-frame period in this two FT(s)11b since the current was passed to EL element 15 by a unit of 1 time in the two-frame period can be passed to an EL element.

[0821] Drawing 314 is in the condition that an applicable pixel is chosen and the current program is performed, in drawing 313. ON state voltage (Vgl) is impressed to gate signal line 17a, and TFT11c and TFT11d turn on. The program current Iw flows toward the source driver (not shown) 14 from TFT11a. OFF state voltage (Vgh) is impressed also to 2 17f 1 and 17f of gate signal lines of gate signal lines, and TFT11f1 and TFT11f2 are OFF states (in addition, in the case of a current mirror, ON state voltage (Vgl) is impressed also to 2 17f 1 and 17f of gate signal lines of gate signal lines, and it is good also considering TFT11f1 and TFT11f2 as an ON state). The program current Iw is supplied from TFT11a for a drive.

[0822] Originally, since TFT 11b1 and TFT11b2 adjoin and they are formed, they should not almost have a property gap. however -- case it formed with the low-temperature polish recon technique -- **** -- Vt electrical potential differences etc. differ. Therefore, the drive TFT11 gate (G) terminal of b1 and TFT 11b2 is carried out in common, even if it impresses the same electrical potential difference to this gate (G) terminal, drive TFT 11b1 differs from the current scale factor which TFT11b2 constitute with TFT11a, and the currents passed to EL element 15 differ. Here, in order to give explanation easy, TFT 11b1 and TFT11b2 have the difference of 3:7, and they explain by setting the current scale factor of TFT11a and TFT11b to 2:1. That is, if program current Iw=10 (muA), TFT 11b1 will supply the current of 3 (muA), and TFT 11b2 will presuppose it that the current of 7 (muA) is supplied. That is, it is program current Iw=Ib1+Ib2=3(muA)+7(muA) =10 (muA).

[0823] If a pixel will be in the condition of not choosing, it will be in the condition (the 1st frame) of drawing 315 (a). OFF state voltage (Vgh) is impressed to gate signal line 17a, and TFT11c and TFT11d turn off. ON state voltage (Vgl) is impressed to 1 17f of gate signal lines at coincidence, and TFT11f1 turns on. Moreover, OFF state voltage (Vgh) is impressed to 2 17f of gate signal lines, and TFT11f2 is an OFF state.

[0824] Therefore, the current Idd1 from drive TFT 11b1 flows to EL element 15. If this current has TFT 11b1 and the same property of TFT11b2, it is Idd1=Iw / 2= 5 (muA). However, TFT 11b1 and the property of TFT11b2 are shifted actually. Here, in order to give explanation easy, it explains as Idd 1= 3 (muA) of TFT 11b1. Therefore, at the 1st frame, EL element 15 emits light with the current of 3 (muA).

[0825] In the 2nd frame next to the 1st frame, actuation explained in drawing 314 is performed again. That is, it is in the condition that an applicable pixel is chosen and the current program is performed. Like the 1st frame, ON state voltage (Vgl) is impressed to gate signal line 17a, and TFT11c and TFT11d turn on. Program current Iw=10 (muA) flows toward the source driver (not shown) 14 from TFT11a.

[0826] If a pixel will be in the condition of not choosing, in the 2nd frame, it will be in the condition of drawing 315 (b). OFF state voltage (Vgh) is impressed to gate signal line 17a, and TFT11c and TFT11d turn off. OFF state voltage (Vgh) is impressed to 1 17f of gate signal lines, and TFT11f1 turns off. Moreover, 17f of gate signal lines, ON state voltage

(Vgl) is impressed to 2, and TFT11f2 is turned on in it.

[0827] Therefore, the current Idd2 from drive TFT 11b2 flows to EL element 15 shortly. If this current had TFT 11b1 and the same property of TFT11b2, the 1st-frame explanation explained the point that it was Idd1=Iw / 2= 5 (muA). However, TFT 11b1 and the property of TFT11b2 are shifted actually. Here, in order to give explanation easy, it explains as Idd 2= 7 (muA) of TFT 11b2. Therefore, at the 2nd frame, EL element 15 emits light with the current of 7 (muA).

[0828] If the above condition is illustrated in the state of a display, it will be in the condition of drawing 312. The number of drawings 312 (a) is the 1st, and drawing 312 (b) is in the condition of the 2nd frame. That is, in the 1st frame, it writes in, the pixel line 871 is chosen and the current of 10 (muA) flows to the source signal line 18. And a current program is carried out at a pixel 16, and the current of 3 (muA) is passed by EL element 15 by TFT 11a1.

[0829] In the 2nd frame, it writes in, the pixel line 871 is chosen and the current of 10 (muA) flows to the source signal line 18 so that it may illustrate to drawing 312 (b). And a current program is carried out at a pixel 16, and the current of 7 (muA) is passed by EL element 15 by TFT 11a2. Therefore, if two frames is averaged, it will be set to (3 (muA)+7 (muA)) / 2= 5 (muA), and one half of the currents of program current Iw=10 (muA) will flow to EL element 15.

[0830] According to the above drive approach, even if two variations of the property of TFT11a for a drive formed in the pixel have occurred, variation is not generated on the average current which flows to EL element 15. That is, the current correctly proportional to the program current Iw (or the same) flows to EL element 15. Therefore, homogeneity image display is realizable.

[0831] In addition, in drawing 313, TFT which supplies the program current Iw is set to TFT11a, it carries out to one per pixel, and TFT which passes a current to EL element 15 is made into TFT one b1 and 2 of TFT11b2. Moreover, TFT 11b1 and TFT1b2 are changed by turns for every frame, and it passes to EL element 15. However, this invention is not limited to this. For example, it is good also considering TFT which makes TFT 11a1 and 2 per pixel of TFT11a2 TFT which supplies the program current Iw, and passes a current to EL element 15 as one of TFT1b. It is because it has the relation of a current mirror.

[0832] Also in this case, actuation is similar to drawing 308. By the 1st frame, program current Iw=10 (muA) is absorbed to the source driver 14. This current Iw is supplied from two TFT(s) 11a1 and TFT11a2. In the 1st frame, 1st TFT 11a1 is chosen, the relation of a current mirror is maintained by this TFT 11a1 and TFT1b, and the current of TFT11b is passed to EL element 15. EL element 15 emits light according to the current of this TFT11b.

[0833] By the 2nd frame, program current Iw=10 (muA) is absorbed to the source driver 14. This current Iw is supplied from two TFT(s) 11a1 and TFT11a2. In the 2nd frame, 2nd TFT 11a2 is chosen, the relation of a current mirror is maintained by this TFT 11a2 and TFT1b, and the current of TFT11b is passed to EL element 15. EL element 15 emits light according to the current of this TFT11b.

[0834] the current (current correctly corresponding to the program current Iw) which does not have variation when two frames is averaged to EL element 15 in the above actuation (a two-frame total -- if) -- ****** -- things are made.

[0835] Although the above example is the case where a pixel configuration is a current program, it cannot be overemphasized that even the pixel configuration of an electrical-potential-difference program absorbs the property variation of two or more drives TFT, and can realize the homogeneity display within a field so that it may illustrate to drawing 316. TFT 11a1 for a drive which passes a current, and switching TFT11f1 which turns a current on and off are formed in EL element 15. Moreover, TFT 11a2 for a drive which passes a current, and switching TFT11f2 which turns a current on and off are formed in EL element 15.

[0836] Actuation is almost the same if the difference of programming drawing 308 etc. on programming with a current and an electrical potential difference is removed. To illustrate to drawing 317, by the 1st frame, a program electrical potential difference is outputted from the source driver 14, and an electrical potential difference is programmed by the capacitor 19. In the 1st frame, the 1st drive TFT 11b1 is chosen so that it may illustrate to drawing 318 (a), and this current is passed to EL element 15. EL element 15 emits light according to the current of this 1st drive TFT 11b1.

[0837] Even the 2nd [at least] frame, like the 1st frame, a program electrical potential difference is outputted from the source driver 14, and an electrical potential difference is held at a capacitor 19. In the 2nd frame, the 2nd drive TFT 11b2 is chosen, and this current is passed to EL element 15. EL element 15 emits light according to the current of this 2nd drive TFT 11b2. Therefore, EL element 15 is turned on with the brightness which averaged the current which two drive TFT11a outputs.

[0838] The same is said of the pixel configuration of the electrical-potential-difference program illustrated by drawing 68 (refer to drawing 319). TFT 11a1 for a drive which passes a current, and switching TFT11f1 which turns a current on and off are formed in EL element 15. Moreover, TFT 11a2 for a drive which passes a current, and switching TFT11f2 which turns a current on and off are formed in EL element 15. Since actuation is the same as that of drawing 316, explanation is omitted. It cannot be overemphasized that TFT11g for reverse bias electrical-potential-difference impression may be added to drawing 309 so that it may illustrate to drawing 320.

[0839] Although it is a matter common to current program methods, such as drawing 1, drawing 21, drawing 43, drawing 71, drawing 40, drawing 69, drawing 70, and drawing 71, there is a trouble that a black display is difficult, by the current program method (it is sharply improvable if this inventions, such as drawing 87 and 88, are carried out, of course.). however -- having -- combining with the following examples is effective. Of course, it cannot be overemphasized that it may not combine with drawing 87 and the example of 88, but the following examples may be carried out independently. For example, even if the white peak current passed to EL element 15 is 2microA, in 64 gradation displays, 1 gradation eye is 2microA/64**30nA. It is rather difficult to carry out the charge and discharge of the parasitic capacitance (stray capacity) 404 of the source signal line 18 etc. to 1H period with this minute current. In addition, in the drawing, although the pixel 16 is formed or arranged in the shape of a matrix, in order to give explanation easy, only 1 pixel is illustrated.

[0840] Since this technical problem is coped with, in this invention, the voltage source 401 for writing the electrical potential difference (current) of black level in the source signal line 18 is formed or arranged. In the voltage source 401, a predetermined electrical potential difference is generated in a DC-DC converter, and specifically, it constitutes so that this electrical potential difference can be impressed with the power-source change means 403 which consists of analog switches etc.

[0841] The signal wave form impressed to the concrete source signal line 18 is shown in drawing 57. TFT11b for a drive (drawing 1 TFT11a) is impressed to the period of t2 of the beginning of 1H period which performs a current program, and OFF or the electrical potential difference (Vb) mostly made a black display is impressed to the source signal line 18. It generates in a voltage source 401 and this electrical potential difference is impressed to the source signal line 18 with the change means 403.

[0842] In a program period, since TFT(s) 11c and 11d are ON states, the electrical potential difference Vb impressed to the source signal line 18 turns into the terminal voltage of a capacitor 19, i.e., the gate terminal voltage of TFT11b. Therefore, a pixel becomes the beginning of 1H period with a black display (astigmatism LGT condition).

[0843] Originally, by black display, the terminal voltage of a capacitor 19 is held for the

image to display as it is. The electrical potential difference Vw (in addition, in the case of the current program, it should be expressed as Iw) of a white display [in a white display] of the image actually displayed after Vb electrical-potential-difference impression is impressed, this electrical potential difference (current) is held at a capacitor 19, and 1H period expires. In addition, in order to give explanation easy here, since the image actually displayed was a white display, it was presupposed that the electrical potential difference Vw (current Iw) of a white display is impressed. However, the electrical potential difference on which it is held with a natural thing at a capacitor 19 in the case of natural drawing is an electrical potential difference between Vw(s) from Vb (current).

[0844] By impressing a signal to the source signal line 18 so that it may illustrate to drawing 57, and driving the gate signal lines 17a and 17b, a good black display can be realized and image display, such as drawing 31, can be carried out.

[0845] When the pixel configuration of drawing 1 also impresses the signal wave form of drawing 57, a good black display is realizable. TFT11a for a drive is impressed to the period of t2 of the beginning of 1H period which performs a current program, and OFF or the electrical potential difference (Vb) mostly made a black display is impressed to the source signal line 18. It generates in a voltage source 401 and this electrical potential difference is impressed to the source signal line 18 with the change means 403.

[0846] In a program period, since TFT(s) 11b and 11c are ON states, the electrical potential difference Vb impressed to the source signal line 18 turns into the terminal voltage of a capacitor 19, i.e., the gate terminal voltage of TFT11a. Therefore, a pixel becomes the beginning of 1H period with a black display (astigmatism LGT condition).

[0847] By black display, the terminal voltage of a capacitor 19 is held for the image it is displayed that explained previously as it is. The electrical potential difference Vw (in addition, in the case of the current program, it should be expressed as Iw) of a white display [in a white display] of the image actually displayed after Vb electrical-potential-difference impression is impressed, this electrical potential difference (current) is held at a capacitor 19, and 1H period expires.

[0848] The voltage source 401 (precharge circuit) illustrated by drawing 40 etc. is a low-temperature polish recon technique etc., and it cannot be overemphasized that you may form directly on a substrate 49. In addition, the electrical potential differences (current) from which generating of light produces EL element 15 since a component configuration differs from an ingredient by R, G, and B differ in many cases (starting electrical potential difference (current)). Since it corresponds to this property, it is desirable to constitute so that a precharge electrical potential difference can be set up according to an individual by R, G, and B. As for one color, it is desirable among the three primary colors to enable it to change at least.

[0849] In addition, it is necessary to make into 1 microseconds or more precharge time amount t2 which impresses Vb. Moreover, as for the precharge time amount t2 which impresses Vb, it is desirable to carry out 1% or more to 10% or less of 1H. It is desirable to carry out 2% or more to 8% or less of 1H still more preferably.

[0850] Moreover, it is desirable to constitute from contents (brightness, definition, etc.) of the display image 21 so that the electrical potential difference to precharge can be changed. For example, that a user pushes an adjustment switch or by turning adjustment BORIUMU, this change is detected and the value of a precharge electrical potential difference (current) is changed. You may constitute so that it may be made to change with the contents of the image to display, and data automatically. For example, a phot sensor detects the strength of external outdoor daylight, and a precharge (discharge) electrical potential difference (current) is adjusted with the detected value. To others, a precharge (discharge) electrical potential difference (current) is adjusted according to the classes (a personal computer image, the screen of daytime, starlit sky, etc.) of image. It opts for adjustment in consideration of the

average brightness of an image, the maximum brightness, the minimum brightness, an animation, a still picture, and luminance distribution.

[0851] Drawing 40 explained the precharge circuit etc. simply. Furthermore, it explains in more detail using drawing 122 etc. In addition, since a discharge and precharge are only the impression directions of potential, they are explained as precharge by making a discharge and precharge into homonymy henceforth.

[0852] Drawing 122 is circuitry which combined the current drive and the electrical-potential-difference drive. The change circuit 1223 is connected to the source signal line 18 with a viewing area. The change circuit 1223 consists of analog switches. An electrical potential difference is impressed to a terminal of the change circuit 1223 (precharge electrical potential difference), and the program current programmed to a pixel is impressed to b terminal.

[0853] 8 bits (256 gradation) IDATA is inputted, the DA translation of this IDATA is carried out by DA converter 1226, and the current output circuit 1222 serves as analog voltage. This analog voltage is impressed to the base terminal of a bipolar transistor (or FET) 1227, and is changed into a current output in an operation of operational amplifier 1224b and resistance 1228. In addition, probably the voltage-current conversion circuit by the transistor 1227, an operational amplifier 1224, etc. will be common, and the engineer of the technical field concerned takes, and the explanation beyond this does not have ****, since it is well-known.

[0854] On the other hand, the voltage-output circuit 1221 consists of buffer circuits by BORIUMU VR 1225 and operational amplifier 1224a. BORIUMU 1225 is common to all source signal lines. The precharge electrical potential difference Vb is determined by adjusting this BORIUMU 1225.

[0855] The precharge electrical potential difference Vb of the beginning of 1 horizontal-scanning period (1H) is impressed. At this time, the change circuit 1223 connected to all source signal lines is connected with Terminal a. Therefore, all the source signal lines 18 are set as the precharge electrical potential difference Vb. Then, the change circuit 1223 is changed to Terminal b, and the current data (256 gradation) corresponding to an image are impressed to the source signal line 18. This current data is written in each pixel 16, and a current flows and emits light to EL element 15 of each pixel.

[0856] In drawing 122, the precharge electrical potential difference Vb was a fixed value. Drawing 123 is a circuitry Fig. which enabled it to take a precharge electrical potential difference 256 values (8 bits). In drawing 123, 8-bit VDATA is inputted and the voltage-output circuit 1221 is changed into analog voltage by DA converter 1226a. The changed analog voltage is inputted into - terminal of operational amplifier 1224c, and it is constituted so that it can adjust to a predetermined electrical potential difference to the reference voltage of VR1225.

[0857] The output of operational amplifier 1224c is impressed to a terminal of change circuit 1223a through buffer amplifier 1224a. On the other hand, the current output is impressed to b terminal of change circuit 1223a.

[0858] VDATA is an electrical potential difference corresponding to IDATA. The precharge electrical potential difference Vb corresponding to VDATA is impressed to the period of 1-10microsec (it is desirable that it is or more 1/100 1/5 or less period of 1H) of the beginning of 1 horizontal-scanning period (1H). At this time, the change circuit 1223 connected to all source signal lines is connected with Terminal a. Therefore, each source signal line 18 is set as the precharge electrical potential difference Vb corresponding to VDATA. The difference with drawing 122 is being able to set the precharge electrical potential difference Vb as each source signal line. That is, the DA converter which carries out the DA translation of the IDATA to each source signal line 18, respectively, and the DA converter which carries out the DA translation of the VDATA are provided. However, it does not limit to providing the

DA converter which carries out the DA translation of the IDATA to each source signal line 18, respectively, and the DA converter which carries out the DA translation of the VDATA. For example, it is because DA circuit is realizable at least one if sample hold of the output is carried out with each source signal line.

[0859] Although the electrical potential difference which changed VDATA is impressed to the period of the beginning of 1H, this electrical-potential-difference value becomes almost equal to the source signal-line potential by the current value corresponding to IDATA impressed henceforth. Therefore, by impressing the electrical potential difference of VDATA, the potential of a source signal line serves as desired value mostly, and is amending to desired value slightly by IDATA. By constituting as mentioned above, the current write-in lack to the source signal line 18 is lost.

[0860] In addition, in drawing 124 (a), although [change circuit 1223a] a terminal and b terminal are changed, it is not limited to this. for example, the drawing 124 (b) -- like, the output of the voltage-output circuit 1221 may be impressed to a terminal, and the output of the current output circuit 1222 may be continuously constituted in the source signal line 18 at a connection condition.

[0861] The flexibility of circuitry improves further by the ability carrying out the output change of DA converter 1226 corresponding to a reference electrical potential difference. When for example, the reference electrical potential difference V is 2.54 (V) as output change can be carried out corresponding to this reference electrical potential difference, what can change an output at 0.01 (V) spacing is said (when the DA converter of 8 bits and 256 gradation is adopted). The reference electrical potential difference V can change an output at 0.02 (V) spacing 5.08 (V).

[0862] That is, the output of a DA converter can be changed in proportion to a reference electrical potential difference by changing a reference electrical potential difference in an instant. Drawing 124 is a circuit block diagram at the time of adopting such a DA converter.

[0863] In drawing 124, the Vref electrical potential difference is impressed to DA converter1226a. A Vref electrical potential difference is outputted from the circuit which consists of RV* resistance which quadrisects Vv electrical potential difference, and switching circuit 1223b. Therefore, a Vref electrical potential difference is changed to four steps by the CVS signal. That is, the output of DA converter 1226a can be changed in four steps in an instant.

[0864] On the other hand, as for DA converter 1226b, the Iref electrical potential difference is impressed. An Iref electrical potential difference is outputted from the circuit which consists of RV* resistance which quadrisects Vi electrical potential difference, and switching circuit 1223c. Therefore, an Iref electrical potential difference is changed to four steps by the CIS signal. That is, the output of DA converter 1226b can be changed in four steps in an instant.

[0865] By constituting, as shown in drawing 124, the current (electrical potential difference) outputted to the source signal line 18 can change now to four steps at the period of 1H. It is impressing a high electrical potential difference (current) first as this operation for a moment, making a high speed reach to desired value by impression, changing into the electrical potential difference (current) of a stationary value after that, and making it desired value etc. That is, the electrical potential difference (current) written in a pixel can be changed into a high speed.

[0866] However, the configuration of drawing 124 becomes what has a quite big circuit scale. The configuration generally illustrated to drawing 125 is enough. The configuration of drawing 124 is constituted so that the voltage-output circuit 1221 can output two electrical-potential-difference values. These two electrical potential differences are electrical potential differences to which one makes image display black. Other one is an electrical potential

difference which makes image display white. The Vdd electrical potential difference of drawing 1 of 6 (V), then a black electrical potential difference is 3(V) -4(V), and, specifically, a white electrical potential difference is 1(V) -2(V). This white electrical potential difference and a black electrical potential difference are adjusted by VR1225, and this electrical potential difference is impressed to switching circuit 1223b through the buffer amplifier 1224a and 1224c. The output of switching circuit 1223b is changed on a VSL electrical potential difference.

[0867] The precharge electrical potential difference Vb (a white electrical potential difference or black electrical potential difference) of the beginning of 1 horizontal-scanning period (1H) is impressed. Each source signal line is connected with the terminal c of change circuit 1223a. Therefore, each source signal line 18 is first set as a white electrical potential difference or a black electrical potential difference by precharge. Then, the change circuit 1223 is changed to Terminal b, and the current data (256 gradation) corresponding to an image are impressed to the source signal line 18. This current data is written in each pixel 16, and a current flows and emits light to EL element 15 of each pixel.

[0868] In the above example, first although [each source signal line 18] set as a white electrical potential difference or a black electrical potential difference by precharge, it is not limited to this. It is more realistic to constitute so that it may precharge when an indicative data (VDATA, IDATA) is beyond a predetermined value, or when it is below a predetermined value.

[0869] Drawing 126 has illustrated the case of 64 gradation displays in order to give explanation easy. In drawing 126 (a), the range of 57 gradation eye to 63 gradation eye (kW) is precharged on a white electrical potential difference. That is, a white electrical potential difference is outputted from the voltage-output circuit 1221 of drawing 125. Moreover, the range of 0 gradation eye to 7 gradation eye (KB) is precharged on a black electrical potential difference. That is, a black electrical potential difference is outputted from the voltage-output circuit 1221 of drawing 125. 8 gradation eye to 56 gradation eye makes the output of the voltage-output circuit 1221 a hi-z state (the switch of change circuit 1223a does not choose Terminal a).

[0870] As mentioned above, a white electrical potential difference is impressed to the gradation which should be considered as a white display, and a black electrical potential difference is impressed to the gradation which should be considered as a black display. Moreover, a gradation display is realizable at high speed and good by not precharging in the part (KM) of halftone.

[0871] In the case of a current program method, it is a black display, and since the program current (current written in a pixel) is as small as 5 or more-nA 20 or less nA, write-in lack occurs. When a black electrical potential difference precharges, an original black display is realizable. However, the display of dark gray may also be written in and lack may occur. In this case, it is effective to precharge the 2nd black in addition to precharge of white and black.

[0872] Drawing 126 (b) is this example. When a black electrical potential difference precharges the range of KB1, an original black display is realizable. And when the 2nd black (gray) precharges the range of KB2, sufficient gradation display is [the part of the gray near black] realizable.

[0873] Here, the black electrical potential difference which the black electrical potential difference on which a Vdd electrical potential difference precharges the range of 6 (V), then KB1 is 3(V) -3.5(V) in the drawing 1 pixel configuration, and more specifically precharges gray of KB2 is 3.5(V) -4.0(V). The white electrical potential difference of the range of KW is 1(V) -2(V). The range of KM does not perform precharge by the electrical potential difference.

[0874] Drawing 126 (b) has illustrated the case of 64 gradation displays in order to give

explanation easy. In drawing 126 (b), the range of 57 gradation eye to 63 gradation eye (kW) is precharged on a white electrical potential difference. The range of 0 gradation eye to 7 gradation eye (KB1) is precharged on a black electrical potential difference. The range of 8 gradation eye to 15 gradation eye (KB2) is precharged on the 2nd black electrical potential difference. 16 gradation eye to 56 gradation eye makes the output of the voltage-output circuit 1221 a hi-z state (the switch of change circuit 1223a does not choose Terminal a).

[0875] As mentioned above, the range of black is divided into two or more range, and a more proper gradation display can be realized by pro charging on an electrical potential difference different, respectively. In addition, although drawing 126 (b) sets the range of black to two, it may not be limited to this, and three or more are sufficient as it. Moreover, precharge may be put in block to all source signal lines, and may be performed. Since what is necessary is just to constitute these circuitry so that three or more buffer amplifier 1224 may be arranged in drawing 125 and three or more switch 1223b can be chosen, it is easy.

[0876] In addition, in drawing 126, the current passed to gradation 0 (black display) at EL element 15 is not 0 (A). Unless it passes EL element 15 beyond a predetermined current, it does not emit light. The current of this range that does not emit light is called the dark current. The dark current has 10 or more-nA about 50 or less nA of pixel sizes by 10000 square mum. A pixel is a black display within the limits of this dark current. Therefore, the current is flowing also with gradation 0. It is necessary to drive with the current which added the dark current as a configuration of a driver IC 14.

[0877] Henceforth, the circuitry illustrated from drawing 122 to drawing 125 is called the output stage circuit 1271. The output stage circuit 1271 is an example of a configuration with common arranging to each source signal line 18 (formation), as illustrated to drawing 127. In drawing 127, although the output stage circuit 1271 is illustrated as formed in the source driver IC 14 formed with the ** silicon chip, it may not be limited to this, and it may be directly formed on a glass substrate 82 at a pixel TFT11 etc. and coincidence. That is, the output stage circuit 1271 may be formed with the approach of forming and growing up into a substrate the seed crystal which the CGS (Continuous Grain Silicon) technical technique which an elevated-temperature polish recon technique, a low-temperature polish recon technique, and Sharp Corp. are developing, and FUJITSU, LTD. are developing, and the technique which forms in a glass substrate etc. the semiconductor circuit formed in the quartz substrate with which Seiko Epson, Inc. is developing by imprint. Moreover, when a substrate 82 is a metal substrate or a semi-conductor substrate, it cannot be overemphasized directly that the output stage circuit 1271 can be formed.

[0878] Moreover, the projection electrode (not shown) which a driver IC 14 uses a plating technique or a nail-head-bonding technique for the signal terminal polar zone of said IC, and consists of gold (Au) with a height of several micrometers to 100 micrometers is formed. Said projection electrode and each signal line are electrically connected through the conductive junctional zone (not shown). A conductive junctional zone is the object with which the epoxy system, the phenol system, etc. were used as base resin as adhesives, and flakes, such as silver (Ag), gold (Au), nickel (nickel), carbon (C), and tin oxide (SnO2), were mixed, or ultraviolet-rays hardening resin. A conductive junctional zone is formed on a projection electrode with techniques, such as an imprint.

[0879] Although it illustrated or explained that drive IC 14 (12) was loaded on a substrate, it does not limit to this. Moreover, IC14 (12) may not be loaded on a substrate 11, but you may connect with a signal line using the polyimide film loading IC etc. using a film carrier technique.

[0880] Drawing 127 is not the thing of a viewing area 21 to limit to this, although it illustrated as the output stage circuit 1271 had been arranged only at the edge on the other hand. For example, driver ICs 14a and 14b may be arranged so that it may illustrate to

drawing 128. Two gate drivers IC 12 are formed in drawing 128. That is, a viewing area consists of 21a and 21b. Thus, if constituted, a separate image can be displayed for viewing areas 21a and 21b.

[0881] Since Screen 21 is divided into two with the configuration of drawing 128, the video signal outputted from the output stage circuit 1271 is good at one half of clock frequency as compared with the case where the number of Screens 21 is one. Moreover, the parasitic capacitance generated in the source signal line 18 etc. is set to one half. Therefore, the burden of the output stage circuit 1271 is set to 1/2x1/2=1/4. Therefore, even if the current outputted from the output stage circuit 1271 is minute, the charge and discharge of the parasitic capacitance of the source signal line 17 can be carried out enough. That is, write-in lack does not occur.

[0882] With the configuration of drawing 128, since screen 21a and screen 21b are divided into two for a viewing area 21 in the center section, a boundary line may be visible in a division location. Drawing 129 copes with this technical problem. Source driver 14a drives the odd-pixel line of a viewing area 21, and source driver 14b drives the even-pixel line of a viewing area 21. Therefore, the boundary line of Screen 21 does not occur.

[0883] In order to improve the lack of a write-in current to a pixel furthermore, in driver ICs 14a and 14b, it is good for the output stage circuit 1271 corresponding to each source signal line 18 to consider as two outputs so that it may illustrate to drawing 130. That is, in output stage circuit 1271a, two output stages (an output stage A, an output stage B) are provided, an output stage A is connected to the odd-pixel line of viewing-area 21a, and the output stage B is connected to the even-pixel line of viewing-area 21a. Moreover, two output stages (an output stage A, an output stage B) are provided also in output stage circuit 1271b, an output stage A is connected to the odd-pixel line of viewing-area 21b, and the output stage B is connected to the even-pixel line of viewing-area 21b. Thus, by constituting, it leads to the ability of still more sufficient current for a source signal line also with a minute current to be passed, and good image display can be realized.

[0884] In addition, in drawing 130 although [the output stage circuit 1271] one source signal line 18 is connected to each pixel, it may not limit to this, a pixel may be made a differential configuration, and you may constitute so that it may drive to each pixel with two source signal lines (it is an object for the bias current + signal currents about the object for bias currents, and the source signal line of another side in one source signal line).

[0885] Drawing 131 is a more concrete configuration-of-module Fig. In drawing 131, 14b is a source driver and 14a is the chip with which the gate driver and the source driver were unified. 14a is driving the gate signal line of a viewing area 21. Driver 14a drives source signal-line 18of viewing-area 21a a. 14b drives source signal-line 18b, and drives viewing-area 21b.

[0886] In addition, drawing 131 is an example, chip 14b also has a gate driver function, and it may constitute it so that gate signal line 17of viewing-area 21b b may be driven. Moreover, although a power source IC 102 and control IC 102 are illustrated as loaded on the printed circuit board 103, they may not be limited to this, and they may be directly formed in a substrate 82. it comes out using the polish recon technique explained above. It cannot be overemphasized that this is applicable also about drawing 10 and drawing 11. Since other configurations are the same as that of drawing 10, drawing 11, drawing 28, drawing 130, etc., explanation is omitted.

[0887] Cong and a roll IC 101 drive both drivers 14a and 14b. The signals (power-source wiring, data wiring, etc.) supplied to driver 14a are supplied through flexible substrate 104c from control IC 101. However, since it is considerably separated from driver 14b of distance, it is first connected to the rear face of a substrate 82 by flexible substrate 104a.

[0888] Drawing 132 is drawing which observed the substrate 82 from the rear face. Signal

wiring (power-source wiring is included) 1321 is formed in the rear face of a substrate 82. Signal wiring 1321 is formed with metallic materials, such as copper, aluminum (aluminum), silver, and silver-palladium, palladium, gold, and aluminum-Mo. Signal wiring 1321 transmits a signal from the edge of a substrate 82 to an edge. Flexible substrate 104b is connected to the end of a substrate 82, and a signal etc. is supplied to driver 14b from this flexible substrate 104b. In addition, drawing 133 is a drawing when seeing from A of drawing 132.

[0889] Although drawing 126 illustrated the pixel configuration of drawing 1, drawing 21, drawing 43, and a current program method like drawing 71 from drawing 40, drawing 57, and drawing 122 and being explained, it does not limit to this. For example, the pixel configuration of electrical-potential-difference program methods, such as drawing 54, drawing 67, drawing 68, drawing 103, drawing 120, and drawing 121, is also effective. In that case, it is necessary to make into an electrical potential difference the signal impressed to b terminal of the change circuit 1223 of drawing 122. This modification is easy, and if it is human being of the technical field concerned, it will be able to respond easily. In an electrical-potential-difference drive, although charge by the parasitic capacitance of the source signal line 18 is not necessarily insufficient, it is because a drive circuit and a digital disposal circuit are simplified and a good black display can be realized by considering as the method which impresses an electrical potential difference at coincidence at two or more pixel line. Moreover, it is because the **** display of an image can be realized and effectiveness is demonstrated by variation absorption of TFT11.

[0890] Therefore, it cannot be overemphasized that the matter explained from drawing 122 in drawing 126 is applicable to all the display panels of this invention, a display, an information display, etc.

[0891] Drawing 41 is the example which used P channels of TFT11 of drawing 1 as N channel. This invention is applicable to various pixel configurations as mentioned above. Also in drawing 41, TFT11d can be turned on and off by controlling the gate signal line 17, and since it cannot be overemphasized that image display, such as drawing 31, is realizable, explanation is omitted. Moreover, since drive waves, such as drawing 33 and drawing 35, are also the same or similar, explanation is omitted. Moreover, it is also effective to set only n TFT(s) 11b and 11c to TFT in drawing 1. a capacitor 19 -- it is because it runs, an electrical potential difference falls and the maintenance property of a capacitor is also improved.

[0892] In addition, drawing 41 is the configuration of providing only a current source 402. That is, the voltage source 401 which precharges is not provided. However, when parasitic capacitance 404 is comparatively small or 1H period has it, even if there is no voltage source 401, a black display can fully be realized. [sufficiently long] Moreover, as drawing 31 etc. explained, when carrying out the perfect non-display field 312, it is that a voltage source 401 is not required in most cases. What is necessary is just to constitute so that it may illustrate to drawing 42 when required.

[0893] Moreover, drawing 43 is the example which used P channels of TFT11 of drawing 21 as N channel. This invention is applicable to various pixel configurations as mentioned above. Also in drawing 43, TFT11e etc. can be turned on and off by controlling the gate signal line 17, and since it cannot be overemphasized that image display, such as drawing 31, is realizable, explanation is omitted. Moreover, since drive waves, such as drawing 33 and drawing 35, are also the same or similar, explanation is omitted.

[0894] As mentioned above, a good black display is realizable by impressing Vb electrical potential difference (Ib current) by the voltage source 401, as explained.

[0895] In addition, if it carries out to N= 10 or more and a high current pulse is impressed to EL element 15, EL terminal voltage will also become high. Moreover, EL element 15 starts by R, G, and B, and an electrical potential difference differs from a gamma curve. Since the

gamma curve is loose, especially B is in the inclination for the terminal voltage of EL element 15 to become high. Power consumption will become large, if a standup electrical potential difference is high and a gamma curve unites terminal voltage with EL element 15 of a loose color (R, G, B color).

[0896] One of the approaches of solving this is the method which separates the cathode shown in drawing 5 by R, G, and B. In addition, it is not necessary to make it respectively different cathode potential by R, G, and B. Especially a gamma curve may separate only the cathode of only one color which has got used from other colors. The configuration which separates Vdd supply voltage as the other approaches as shown in drawing 58 is also effective. That is, it is the configuration which sets the Vdd power source of R color to VddR, sets the Vdd power source of G color to VddG, and sets the Vdd power source of B color to VddB. Thus, by dissociating, each RGB can be adjusted with another power source, and even if the terminal voltage of EL element 15 of RGB differs, the increment in power consumption becomes small.

[0897] In addition, it is not necessary to make it respectively different Vdd potential by R, G, and B. Especially a gamma curve may separate only Vdd of only one color which has got used from other colors. Moreover, you may combine with the configuration of drawing 5 so that it may illustrate to drawing 59. That is, it considers as respectively different cathode potential (for VsR and G pixels, VsG and B pixels are [R pixels] VsB) by R, G, and B which are the method separated by R, G, and B. Especially a gamma curve may separate only the cathode potential of only one color which has got used from other colors. Furthermore, Vdd supply voltage is separated. It is the configuration which sets the Vdd power source of R color to VddR, sets the Vdd power source of G color to VddG, and sets the Vdd power source of B color to VddB. It is not necessary to make it respectively different Vdd potential by R, G, and B also in this case. Especially a gamma curve may separate only Vdd of only one color which has got used from other colors.

[0898] In addition, although the pixel 16 was considered as the configuration of drawing 1 in drawing 58 and drawing 59, it is not limited to this and it cannot be overemphasized that the configuration of drawing 78 etc. may be used from drawing 21, drawing 22, drawing 43, drawing 44, drawing 41, drawing 42, drawing 54, and drawing 67.

[0899] Although the current impressed to the technical problem of this invention at EL element 15 is instant-like, there is a problem that it is N times larger as compared with the former. If a current is large, the life of an EL element may be reduced. In order to solve this technical problem, it is effective to impress the reverse bias electrical potential difference Vm to EL element 15.

[0900] Hereafter, the approach of impressing a reverse bias is explained. In order to impress a reverse bias, in the configuration of drawing 1, it is necessary to control the gate terminal of TFT11b and TFT11c according to an individual. That is, it is necessary to make TFT11b and TFT11c turn on and off according to an individual. This control approach is explained using drawing 52.

[0901] First, TFT11c is turned on and TFT11d is made to turn on, as shown in drawing 52 (a) (also unite and refer to drawing 1). And it is impressed by a terminal of the reverse bias electrical potential difference Vm and EL element 15. Vm electrical potential difference is an electrical potential difference lower than Vs. Vm electrical potential difference is an electrical potential difference with the low value within 15 (V) more than 5 (V) from Vs.

[0902] In addition, as for the signal line 17 which supplies a reverse bias electrical potential difference, it is desirable to form in parallel with the source signal line 18. Since it can form with low resistance wiring and there is no cross with the source signal line 18, it is hard to generate coupling of a reverse bias signal line and the source signal line 18. In addition, of course, the signal line 17 which supplies a reverse bias electrical potential difference may be

formed in parallel with the gate signal line 17.

[0903] When EL element 15 lights up, the high electrical potential difference within 15 (V) is impressed to a terminal more than 5 (V) to Vs. That is, with Vm electrical potential difference, an absolute value impresses a polar reverse electrical potential difference equally ideally to the electrical potential difference impressed when EL element 15 is on. Actually, equally [an absolute value], since impression is difficult in a polar reverse electrical potential difference, one 2 to 3 times the electrical potential difference of this is impressed with reversed polarity. EL element 15 stops almost deteriorating by impressing a reverse bias as mentioned above.

[0904] Next, TFT11d is turned off and TFT11b is made to turn on, as shown in drawing 52 (b). And the black electrical potential difference Vb is written in a capacitor 19. Drawing 57 explains this actuation. Next, as shown in drawing 52 (c), the on-off condition of TFT11 is in the same condition as drawing 52 (b), and writes the image display electrical potential difference (current) from a current source 402 in a capacitor 19. Drawing 57 also explains this actuation. Turn off TFT(s) 11b and 11c and TFT11d is made to turn on, a current is passed to EL element 15 and it is made to turn on EL element 15 finally, as shown in drawing 52 (d).

[0905] The above actuation is shown in drawing 15. The reverse bias electrical potential difference Vm is impressed to the source signal line 18 in t 1 hour of 1H period, and Vb electrical potential difference is impressed to the t2 next period, and image data Vw (Iw) is impressed during t tertiary stage. Since drawing 52 explains other actuation and drawing 31, such as the drive approach, drawing 33, etc. explain it, it omits explanation.

[0906] In case the current of the source signal line 18 is crowded with the configuration of drawing 121 drawing 52 for a pixel 16 from drawing 119, a reverse current flows to EL element 15. Therefore, when EL elements 15 are organic electroluminescence devices, it becomes possible like [at the time of impressing reverse voltage] to make late electrochemical degradation by the oxidation reduction reaction of an organic molecule etc.

[0907] The energy diagram of the three-layer mold organic light emitting device which consists of an anode plate / electron hole transportation layer / luminous layer / an electron transport layer / cathode is shown in drawing 102. The behavior of the positive/negative carrier at the time of luminescence is expressed in drawing 102 (a). An electron hole is also injected into an electron hole transportation layer from an anode plate (anode) at the same time an electron is injected into an electron transport layer from cathode (cathode). The poured-in electron and an electron hole are moved to a counter electrode by impression electric field. In that case, a trap is carried out into an organic layer, or a carrier is accumulated in the difference of the energy level in a luminous layer interface like a twist.

[0908] If space charge is accumulated into an organic layer, causing the fall of brightness and the rise of the driver voltage at the time of a constant current drive by deterioration of membraneous quality is known for the radical anion molecule or radical cation molecule with which it was oxidized or returned and the molecule was generated being unstable. In order to prevent this, device structure is changed as an example and reverse voltage is impressed.

[0909] Since a reverse current is impressed in drawing 102 (b), the electron and electron hole which were poured in are drawn out to cathode and an anode plate, respectively. Thereby, the space charge formation in an organic layer is canceled, and it becomes possible to lengthen a life by suppressing electrochemical degradation of a molecule.

[0910] In addition, although drawing 102 explained the three-layer mold component, also in the multilayer mold component more than a four-layer mold, and the component below a two-layer mold, it is same that electrochemical degradation of the organic film takes place by the electron and electron hole which were poured in from the electrode. Therefore, it becomes possible not to be based on the number of layers but to lengthen a life by this example. Since

electrochemical degradation of a molecule is similarly produced in the component which mixed two or more ingredients with one layer, it is effective.

[0911] Even if the description in this invention gives the function to pass the bias current for preventing the wave provincial accent by the stray capacity which gives the function which prevents degradation of an organic molecule in this way, and is parasitic on a source signal line, it is being able to display without making a transistor count required for a pixel increase. That is, since that it is not necessary to increase the number of the transistors for passing a reverse current does not need to lower the numerical aperture of each pixel of a display, it serves as an advantage.

[0912] The impression effectiveness of the reverse bias electrical potential difference Vm is explained in drawing 109. Drawing 109 shows the luminescence brightness of EL element 15 when driving with a predetermined current, and the terminal voltage of an EL element. In drawing 109, the dotted-line continuous line b shows the terminal voltage of EL element 15 when impressing the reverse bias electrical potential difference Vm to EL element 15. The alternate long and short dash line c shows the terminal voltage of EL element 15 when not impressing a reverse bias electrical potential difference to EL element 15. Moreover, the continuous line a shows the luminescence brightness ratio (ratio when setting initial brightness to 1) of EL element (dotted line a) 15 when impressing a reverse bias electrical potential difference to EL element 15.

[0913] In drawing 109, an EL element is R luminescence and, specifically, is the case where a current drive is carried out in current density 100A / square meter. Sample B is impressing the current of current density 100A / square meter continuously between time amount t. Terminal voltage became high in lighting time amount 1500 hours, the brightness fall was carried out rapidly, and only about 15% of brightness was obtained to initial brightness after 2500-hour progress.

[0914] Sample A carried out the 30Hz pulse drive, the current of current density 200A / square meter was impressed to the half time amount t2, and it impressed the reverse bias electrical potential difference -14 (V) to the time amount t1 of a sink and the one half of the second half (that is, the average luminescence brightness per unit time amount is the same with Samples A and B). The lighting time amount from which Sample A does not almost have change of the terminal voltage of EL element 15 as a dotted line b shows, and brightness becomes 50% was 4000 hours.

[0915] Thus, there is no increment in the terminal voltage of EL element 15 in impressing the reverse bias electrical potential difference Vm, and the reduction rate of luminescence brightness also decreases. Therefore, the long lasting drive of EL element 15 is realizable.

[0916] Drawing 108 shows change of the reverse bias electrical potential difference Vm and the terminal voltage of EL element 15. This terminal voltage is a time of impressing the rated current to EL element 15. Although drawing 108 was the case where the currents passed to EL element 15 were current density 100A / square meter, the inclination of drawing 108 did not almost have a difference with the case of current density 50-100A / square meter. Therefore, it is presumed that it is applicable with the current density of the large range.

[0917] An axis of ordinate is a ratio with the terminal voltage of 2500 hours after to the terminal voltage of early EL element 15. For example, in elapsed time 0 hour, terminal voltage when the current of current density 100A / square meter impresses sets to 8 (V), and the terminal voltage of 10 (V), then a terminal voltage ratio when the current of current density 100A / square meter impresses is 10 / 8= 1.25 in elapsed time 2500 hours.

[0918] An axis of abscissa is the ratio of the reverse bias electrical potential difference Vm and the rated terminal voltage V0 to the product of time amount t1 which impressed the reverse bias electrical potential difference to one period. For example, it is t1=0.5 if the time amount which is 60Hz (there is especially no semantics in 60Hz), and impressed the reverse

bias electrical potential difference Vm is 1/2 (one half). Moreover, in elapsed time 0 hour, terminal voltage (rated terminal voltage) when the current of current density 100A / square meter impresses sets to 8 (V), and is set to 8 (V), then | reverse bias electrical-potential-difference xt1|/(rated terminal voltage xt2) =|-8(V) x0.5|/(8(V) x0.5) =1.0 in the reverse bias electrical potential difference Vm.

[0919] According to drawing 108, | reverse bias electrical-potential-difference xt1|/(rated terminal voltage xt2) of change of a terminal voltage ratio is lost or more by 1.0 (it does not change from early rated terminal voltage). The effectiveness by impression of the reverse bias electrical potential difference Vm is often demonstrated. However, | reverse bias electrical-potential-difference xt1|/(rated terminal voltage xt2) tends to increase a terminal voltage ratio or more by 1.75. Therefore, | reverse bias electrical-potential-difference xt1|/(rated terminal voltage xt2) is good to determine that the magnitude and the impression time amount ratio t1 (or ratio of t2, or t1 and t2) of the reverse bias electrical potential difference Vm will carry out to 1.0 or more. Moreover, | reverse bias electrical-potential-difference xt1|/(rated terminal voltage xt2) is good preferably to determine like that magnitude, the impression time amount ratio t1, etc. of the reverse bias electrical potential difference Vm will become 1.75 or less.

[0920] However, to perform a bias drive, it is necessary to impress a reverse bias Vm and the rated current by turns. If it is going to make equal average luminance per unit time amount with Samples A and B as shown in drawing 109, to impress a reverse bias electrical potential difference, it is necessary to pass a current high in instant as compared with the case where it does not impress. Therefore, the terminal voltage of EL element 15 in the case (the sample A of drawing 109) of impressing the reverse bias electrical potential difference Vm also becomes high.

[0921] However, in drawing 108, it considers as the terminal voltage (that is, terminal voltage which turns on EL element 15) with which are satisfied of average luminance with the rated terminal voltage V0 also by the drive approach of impressing a reverse bias electrical potential difference (according to the example of this specification, it is terminal voltage when the current of current density 200A / square meter impresses.). However, since it is 1/2 duty, the average luminance of one period turns into brightness in current density 200A / square meter.

[0922] The above matter assumes white raster display for EL element 15 (when maximum current is being impressed to the EL element of the whole screen). However, when performing graphic display of EL display, it is natural drawing and a gradation display is performed. Therefore, it is the white peak current (current which flows by the maximum white display.) of EL element 15 continuously. By the example of this specification, the current of average current density 100A / square meter is not flowing.

[0923] The current (flowing current) generally impressed to each EL element 15 when performing graphic display is the white peak current (current which flows at the time of rated terminal voltage.). According to the example of this specification, it is about 0.2 times the current of current density 100A / square meter.

[0924] Therefore, in the example of drawing 108, when performing graphic display, 0.2 shall be applied to the value of an axis of abscissa. Therefore, | reverse bias electrical-potential-difference xt1|/(rated terminal voltage xt2) is good to determine that the magnitude and the impression time amount ratios t1 of the reverse bias electrical potential difference Vm (or ratio of t2, or t1 and t2 etc.) will carry out to 0.2 or more. Moreover, | reverse bias electrical-potential-difference xt1|/(rated terminal voltage xt2) is good preferably to determine like that magnitude, the impression time amount ratio t1, etc. of the reverse bias electrical potential difference Vm will become less than [1.75x0.2=0.35].

[0925] That is, in the axis of abscissa (| reverse bias electrical-potential-difference xt1|/(rated terminal voltage xt2)) of drawing 108, it is necessary to set the value of 1.0 to 0.2. Therefore,

an image is displayed on a display panel (this busy condition will be usual.). When always not displaying a white raster, it is made to impress the reverse bias electrical potential difference Vm predetermined time t1 so that | reverse bias electrical-potential-difference xt1|/(rated terminal voltage xt2) may become larger than 0.2. Moreover, even if the value of | reverse bias electrical-potential-difference xt1|/(rated terminal voltage xt2) becomes large, the increment in a terminal voltage ratio is not large so that it may illustrate in drawing 108. Therefore, what is necessary is for a upper limit to also take carrying out white raster display into consideration, and just to make it the value of | reverse bias electrical-potential-difference xt1|/(rated terminal voltage xt2) satisfy 1.75 or less.

[0926] Hereafter, the reverse bias method of this invention is explained, referring to a drawing. In addition, this invention is based on impressing the reverse bias electrical potential difference Vm (current) to the period when the current is not flowing to EL element 15. However, it does not limit to this. For example, the reverse bias electrical potential difference Vm may be compulsorily impressed to EL element 15 in the condition that the current is flowing. In addition, in this case, to EL element 15, a current will not flow as a result, but it will be in the astigmatism LGT condition (black display condition). Moreover, although this invention explains impressing the reverse bias electrical potential difference Vm mainly with the pixel configuration of a current program as a core, it is not limited to this. For example, TFT11e is made to turn off in drawing 103, and if it is made the configuration which impresses the reverse bias electrical potential difference Vm to the anode of EL element 15 like drawing 90, the impression of the reverse bias electrical potential difference Vm explained below is easily realizable also with the pixel configuration of an electrical-potential-difference program method. It can carry out and backlash can demonstrate the effectiveness explained in drawing 108 etc.

[0927] Drawing 90 arranges or forms switching TFT11g which impresses the reverse bias electrical potential difference Vm to the pixel configuration of drawing 1 (a). The gate terminal of TFT11g is connected to 17d of gate signal lines for control. Vm electrical potential difference is impressed to the anode of EL element 15 by making TFT11g turn on.

[0928] Drawing 90 is the explanatory view of the drive approach of the reverse bias electrical-potential-difference impression method of this invention. First, if an electrical potential difference Vgl is impressed to gate signal line 17a as shown in drawing 107 (a1), TFT(s) 11b and 11c turn on. Then, as shown in drawing 107 (a2), the program current Iw flows from the source driver 14 to TFT11c etc., and a current program is carried out at a capacitor 19. In addition, although it does not limit N times, in order to give explanation easy here, a N times as many current as this shall be programmed, and only the period of 1 F/N shall pass Current Id to EL element 15.

[0929] Next, an electrical potential difference Vgh is impressed to gate signal line 17b, and TFT(s) 11b and 11c turn off so that it may illustrate to drawing 107 (b1). If an electrical potential difference Vgl is impressed to coincidence (it does not limit to coincidence) at gate signal line 17b, TFT11d turns on. Then, as shown in drawing 107 (c2), the current Id by which the current program of the power source Vdd was carried out through TFT11a flows to EL element 15. Therefore, EL element 15 emits light so that it may illustrate to drawing 107 (c1). This luminescence brightness will emit light by one about N times the brightness of this, if the conversion efficiency of a program is 100%.

[0930] A luminescence period is 1 F/N. TFT11d of the remaining periods of 1F (1-1/N) is an OFF state, and EL element 15 serves as an astigmatism LGT (black display). Since a current does not flow at all to EL element 15, a black display can realize a perfect black display. Moreover, at the time of luminescence, since the white peak current is large, luminescence brightness is also high. Therefore, by the drive approach of this invention, a high contrast display is very realizable.

[0931] If it indicates to implementation use by black when a 1 time as many current as this is passed to all the periods of 1F at EL element 15 (the conventional drive method), it is necessary to program a black display current to a capacitor 19. However, by the current drive method, since the current value at the time of a black display is small, popularity is greatly won with the effect of parasitic capacitance, and the technical problem that sufficient resolution does not come out occurs. Moreover, the technical problem that a black float is generated is also generated. Moreover, it runs from the gate signal line 17, and is influenced of an electrical potential difference. Also in a black display, by these technical problems, EL element 15 will be in a fine lighting condition. It carries out and contrast gets very bad [backlash].

[0932] By the method of this invention, as for the period of 1F (1-1/N), a current does not flow to EL element 15 completely. Therefore, a perfect black display is realizable. That is, a black float is not generated. Therefore, even if it does not perform precharge for the black display explained by drawing 52 etc., a high contrast display is realizable.

[0933] In addition, it cannot be overemphasized that methods, such as drawing 52, may be added and carried out, of course to the method explained by drawing 90 etc. Moreover, it is effective of the pixel configuration of electrical-potential-difference programs, such as drawing 54, drawing 67, and drawing 103, similarly that a high contrast display is realizable. By carrying out one F/N pulse drive, it is because a current does not flow at all to EL element 15 but the period of 1F (1-1/N) can realize a high contrast display. Of course, the good movie display by making image display into an intermission is realizable.

[0934] Moreover, when acting in the direction to which the current to which it runs depending on a pixel configuration, and an electrical potential difference flows to EL element 15 is made to increase, the white peak current increases and the feeling of contrast of image display increases. Therefore, good image display is realizable.

[0935] ON state voltage is impressed to 17d of gate signal lines, and TFT11g is made to turn on so that it may illustrate to drawing 107 (d1). At this time, TFT11d carries out an OFF state. By making TFT11g turn on, it is the anode (in addition depending on a pixel configuration, the reverse bias electrical potential difference Vm may be impressed to the cathode of EL element 15) of EL element 15. Moreover, the reverse bias electrical potential difference Vm is the reverse bias electrical potential difference Vm (it can express, even if the reverse bias current Im flows.) for there being a case of the electrical potential difference of straight polarity. It is because it can be considered in circuit that EL element 15 is a capacitor, so a current flows in alternating current by impression of a reverse bias electrical potential difference. Moreover, it is because the accumulated charge discharges. It is impressed. The time amount t1 to impress is constituted so that the condition of drawing 108 may be satisfied (drawing 107 (d2)).

[0936] As for the period which impresses the reverse bias electrical potential difference Vm, it is desirable to consider as the period when Current Id is not flowing to EL element 15. It is because a reverse bias electrical potential difference and a short condition will occur if Id is flowing (it can do).

[0937] in addition, the thing limited to this although the period which impresses the reverse bias electrical potential difference Vm in drawing 107 (d1) was made into one of 1F places -- it is not -- two or more division (for example, the reverse bias electrical potential difference Vm is impressed to EL element 15 in 2 times or more or 3 steps or more at the period of 1F) -- you may carry out.

[0938] This control is easy. It is because what is necessary is just to impress an on-off electrical potential difference to 17d of gate signal lines to the timing of arbitration among the periods which are impressing OFF state voltage to gate signal line 17b. What is necessary is just to make it total of such ON time amount become t 1 hour explained in drawing 108.

[0939] Moreover, the period of period 1F (1-1/N) which do not pass a current to EL element 15 may be divided at two or more periods. Generating of a flicker is controlled by dividing. What is necessary is just to impress the reverse bias electrical potential difference Vm to the period, when the period of period 1F (1-1/N) which do not pass a current to EL element 15 is divided at two or more periods. However, it is not necessary to impress the reverse bias electrical potential difference Vm to all of period 1F (1-1/N) which do not pass a current to divided EL element 15.

[0940] It is necessary to amend the contents explained in drawing 108 by the drive approach that do not impress a reverse bias electrical potential difference as shown in drawing 109, and the current is not flowing to EL element 15, either (or supplement). That is, the time amount t1 explained in drawing 108 is the time amount which impressed the reverse bias electrical potential difference Vm. Moreover, time amount t2 is the time amount which impressed the current to EL element 15.

[0941] In addition, the reverse bias electrical potential difference Vm does not need to be a fixed value in direct current. It is impressing by Vm=-8 (V) immobilization. That is, the reverse bias electrical potential difference Vm is good also as a signal of a teeth-of-a-saw wave, and good also as a wave-like pulse signal. Moreover, the signal wave form of a sine wave is sufficient. In this case, with a reverse bias electrical potential difference, it considers as the thing which integrated with the wave, or actual value. Moreover, what is necessary is just to set to t1 time amount to which makes thing actual value which integrated with Vm electrical potential difference a square wave form, and it is supposed that this square wave form was impressed, although the impression time amount t1 also becomes indefinite.

[0942] For example, the wave of a reverse bias electrical potential difference presupposes that it is the voltage waveform (3 square-shape wave) illustrated to drawing 115 (a). Suppose that a maximum amplitude value is 16 (V) and impression time amount is t1=100 (microsecondec). In this case, 8 (V) and impression time amount have a maximum amplitude value equivalent to the voltage waveform of t1=100 (microsecondec) so that it may illustrate to drawing 115 (b).

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] The circuitry Fig. of the display panel of this invention
[Drawing 2] The circuitry Fig. of the display of this invention
[Drawing 3] The explanatory view of the display of this invention
[Drawing 4] The sectional view of the display of this invention
[Drawing 5] The explanatory view of the display of this invention
[Drawing 6] The explanatory view of the display of this invention
[Drawing 7] The sectional view of the display of this invention
[Drawing 8] The sectional view of the display of this invention
[Drawing 9] The sectional view of the display of this invention
[Drawing 10] The block diagram of the display of this invention
[Drawing 11] The block diagram of the display of this invention
[Drawing 12] The circuitry Fig. of the conventional display panel
[Drawing 13] The explanatory view of the display panel of this invention
[Drawing 14] The explanatory view of the display of this invention
[Drawing 15] The explanatory view of the display of this invention
[Drawing 16] The explanatory view of the data transmission approach of the indicating equipment of this invention
[Drawing 17] The explanatory view of the data transmission approach of the indicating

equipment of this invention

[Drawing 18] The explanatory view of the data transmission approach of the indicating equipment of this invention

[Drawing 19] The top view of the information display of this invention

[Drawing 20] The explanatory view of the information display of this invention

[Drawing 21] The explanatory view of the display panel of this invention

[Drawing 22] The explanatory view of the display panel of this invention

[Drawing 23] The explanatory view of the manufacture approach of the display panel of this invention

[Drawing 24] The explanatory view of the manufacture approach of the display panel of this invention

[Drawing 25] The sectional view of the display panel of this invention

[Drawing 26] The explanatory view of the display panel of this invention

[Drawing 27] The explanatory view of the display panel of this invention

[Drawing 28] The explanatory view of the display panel of this invention

[Drawing 29] The explanatory view of the display panel of this invention

[Drawing 30] The explanatory view of the display panel of this invention

[Drawing 31] The explanatory view of the drive approach of the display panel of this invention

[Drawing 32] The explanatory view of the drive approach of the display panel of this invention

[Drawing 33] The explanatory view of the drive approach of the display panel of this invention

[Drawing 34] The explanatory view of the drive approach of the display panel of this invention

[Drawing 35] The circuit block diagram of the display panel of this invention

[Drawing 36] The explanatory view of the drive approach of the display panel of this invention

[Drawing 37] The explanatory view of the drive approach of the display panel of this invention

[Drawing 38] The explanatory view of the drive approach of the display panel of this invention

[Drawing 39] The explanatory view of the drive approach of the display panel of this invention

[Drawing 40] The explanatory view of the display panel of this invention

[Drawing 41] The explanatory view of the display panel of this invention

[Drawing 42] The explanatory view of the display panel of this invention

[Drawing 43] The explanatory view of the display panel of this invention

[Drawing 44] The explanatory view of the display panel of this invention

[Drawing 45] The sectional view of the viewfinder of this invention

[Drawing 46] The perspective view of the video camera of this invention

[Drawing 47] The perspective view of the electronic camera of this invention

[Drawing 48] The explanatory view of television of this invention

[Drawing 49] The explanatory view of television of this invention

[Drawing 50] The explanatory view of the drive approach of the display panel of this invention

[Drawing 51] The explanatory view of the drive approach of the display panel of this invention

[Drawing 52] The explanatory view of the drive approach of the display panel of this invention

[Drawing 53] The explanatory view of the display panel of this invention
[Drawing 54] The explanatory view of the display panel of this invention
[Drawing 55] The explanatory view of the display panel of this invention
[Drawing 56] The explanatory view of the drive approach of the display panel of this invention
[Drawing 57] The explanatory view of the drive approach of the display panel of this invention
[Drawing 58] The explanatory view of the display panel of this invention
[Drawing 59] The explanatory view of the display panel of this invention
[Drawing 60] The circuit block diagram of the display panel of this invention
[Drawing 61] The explanatory view of the drive approach of the display panel of this invention
[Drawing 62] The explanatory view of the drive approach of the display panel of this invention
[Drawing 63] The explanatory view of the drive approach of the display panel of this invention
[Drawing 64] The explanatory view of the drive approach of the display panel of this invention
[Drawing 65] The explanatory view of the drive approach of the display panel of this invention
[Drawing 66] The explanatory view of the drive approach of the display panel of this invention
[Drawing 67] The explanatory view of the display panel of this invention
[Drawing 68] The explanatory view of the display panel of this invention
[Drawing 69] The explanatory view of the display panel of this invention
[Drawing 70] The explanatory view of the display panel of this invention
[Drawing 71] The explanatory view of the display panel of this invention
[Drawing 72] The explanatory view of the display panel of this invention
[Drawing 73] The explanatory view of the display panel of this invention
[Drawing 74] The circuit block diagram of the display panel of this invention
[Drawing 75] The explanatory view of the display panel of this invention
[Drawing 76] The explanatory view of the display panel of this invention
[Drawing 77] The explanatory view of the display panel of this invention
[Drawing 78] The explanatory view of the display panel of this invention
[Drawing 79] The explanatory view of the display panel of this invention
[Drawing 80] The explanatory view of the display panel of this invention
[Drawing 81] The explanatory view of the display panel of this invention
[Drawing 82] The explanatory view of the display panel of this invention
[Drawing 83] The explanatory view of the display panel of this invention
[Drawing 84] The circuit block diagram of the display panel of this invention
[Drawing 85] The explanatory view of the information display of this invention
[Drawing 86] The explanatory view of the information display of this invention
[Drawing 87] The explanatory view of the drive approach of the display panel of this invention
[Drawing 88] The explanatory view of the drive approach of the display panel of this invention
[Drawing 89] The explanatory view of the display panel of this invention
[Drawing 90] The explanatory view of the display panel of this invention
[Drawing 91] The explanatory view of the display panel of this invention
[Drawing 92] The explanatory view of the display panel of this invention

[Drawing 93] The explanatory view of the display panel of this invention
[Drawing 94] The explanatory view of the display panel of this invention
[Drawing 95] The explanatory view of the display panel of this invention
[Drawing 96] The explanatory view of the display panel of this invention
[Drawing 97] The explanatory view of the display panel of this invention
[Drawing 98] The explanatory view of the display panel of this invention
[Drawing 99] The explanatory view of the display panel of this invention
[Drawing 100] The explanatory view of the display panel of this invention
[Drawing 101] The explanatory view of the display panel of this invention
[Drawing 102] The explanatory view of the display panel of this invention [drawing 103] The explanatory view of the display panel of this invention
[Drawing 104] The explanatory view of the drive approach of the display panel of this invention
[Drawing 105] The explanatory view of the drive approach of the display panel of this invention
[Drawing 106] The explanatory view of the drive approach of the display panel of this invention
[Drawing 107] The explanatory view of the drive approach of the display panel of this invention
[Drawing 108] The explanatory view of the drive approach of the display panel of this invention
[Drawing 109] The explanatory view of the drive approach of the display panel of this invention
[Drawing 110] The explanatory view of the drive approach of the display panel of this invention
[Drawing 111] The explanatory view of the display panel of this invention
[Drawing 112] The explanatory view of the display panel of this invention
[Drawing 113] The explanatory view of the display panel of this invention
[Drawing 114] The explanatory view of the display panel of this invention
[Drawing 115] The explanatory view of the display panel of this invention
[Drawing 116] The explanatory view of the pixel configuration of the display panel of this invention
[Drawing 117] The explanatory view of the pixel configuration of the display panel of this invention
[Drawing 118] The explanatory view of the pixel configuration of the display panel of this invention
[Drawing 119] The explanatory view of the pixel configuration of the display panel of this invention
[Drawing 120] The explanatory view of the pixel configuration of the display panel of this invention
[Drawing 121] The explanatory view of the pixel configuration of the display panel of this invention
[Drawing 122] The explanatory view of the drive approach of the display panel of this invention
[Drawing 123] The explanatory view of the drive approach of the display panel of this invention
[Drawing 124] The explanatory view of the drive approach of the display panel of this invention
[Drawing 125] The explanatory view of the drive approach of the display panel of this invention

[Drawing 126] The explanatory view of the drive approach of the display panel of this invention

[Drawing 127] The explanatory view of the display panel of this invention

[Drawing 128] The explanatory view of the display panel of this invention

[Drawing 129] The explanatory view of the display panel of this invention

[Drawing 130] The explanatory view of the display panel of this invention

[Drawing 131] The explanatory view of the display panel of this invention

[Drawing 132] The explanatory view of the display panel of this invention

[Drawing 133] The explanatory view of the display panel of this invention

[Drawing 134] The explanatory view of the drive approach of the display panel of this invention

[Drawing 135] The explanatory view of the drive approach of the display panel of this invention

[Drawing 136] The explanatory view of the drive approach of the display panel of this invention

[Drawing 137] The explanatory view of the drive approach of the display panel of this invention

[Drawing 138] The explanatory view of the drive approach of the display panel of this invention

[Drawing 139] The explanatory view of the drive approach of the display panel of this invention

[Drawing 140] The explanatory view of the drive approach of the display panel of this invention

[Drawing 141] The explanatory view of the drive approach of the display panel of this invention

[Drawing 142] The explanatory view of the drive approach of the display panel of this invention

[Drawing 143] The explanatory view of the drive approach of the display panel of this invention

[Drawing 144] The explanatory view of the drive approach of the display panel of this invention

[Drawing 145] The explanatory view of the drive approach of the display panel of this invention

[Drawing 146] The explanatory view of the drive approach of the display panel of this invention

[Drawing 147] The explanatory view of the drive approach of the display panel of this invention

[Drawing 148] The explanatory view of the drive circuit of the display panel of this invention

[Drawing 149] The explanatory view of the drive circuit of the display panel of this invention

[Drawing 150] The explanatory view of the drive circuit of the display panel of this invention

[Drawing 151] The explanatory view of the drive approach of the display panel of this invention

[Drawing 152] The explanatory view of the drive approach of the display panel of this invention

[Drawing 153] The explanatory view of the drive approach of the display panel of this invention

[Drawing 154] The explanatory view of the drive approach of the display panel of this invention

[Drawing 155] The explanatory view of the drive approach of the display panel of this invention

[Drawing 156] The explanatory view of the drive approach of the display panel of this invention

[Drawing 157] The explanatory view of the drive approach of the display panel of this invention

[Drawing 158] The explanatory view of the drive approach of the display panel of this invention

[Drawing 159] The explanatory view of the drive approach of the display panel of this invention

[Drawing 160] The explanatory view of the drive approach of the display panel of this invention

[Drawing 161] The explanatory view of the drive approach of the display panel of this invention

[Drawing 162] The explanatory view of the drive approach of the display panel of this invention

[Drawing 163] The explanatory view of the drive approach of the display panel of this invention

[Drawing 164] The explanatory view of the drive approach of the display panel of this invention

[Drawing 165] The explanatory view of the drive approach of the display panel of this invention

[Drawing 166] The explanatory view of the drive approach of the display panel of this invention

[Drawing 167] The explanatory view of the drive approach of the display panel of this invention

[Drawing 168] The explanatory view of the display panel of this invention
[Drawing 169] The explanatory view of the display panel of this invention
[Drawing 170] The explanatory view of the display panel of this invention
[Drawing 171] The explanatory view of the display panel of this invention
[Drawing 172] The explanatory view of the display panel of this invention
[Drawing 173] The explanatory view of the display panel of this invention
[Drawing 174] The explanatory view of the display panel of this invention
[Drawing 175] The explanatory view of the display panel of this invention
[Drawing 176] The explanatory view of the display panel of this invention
[Drawing 177] The explanatory view of the manufacture approach of the display panel of this invention
[Drawing 178] The explanatory view of the display panel of this invention
[Drawing 179] The explanatory view of the display panel of this invention
[Drawing 180] The explanatory view of the display panel of this invention
[Drawing 181] The explanatory view of the display panel of this invention
[Drawing 182] The explanatory view of the display panel of this invention
[Drawing 183] The explanatory view of the display panel of this invention
[Drawing 184] The explanatory view of the display panel of this invention
[Drawing 185] The explanatory view of the display panel of this invention
[Drawing 186] The explanatory view of the display panel of this invention
[Drawing 187] The explanatory view of the display panel of this invention
[Drawing 188] The explanatory view of the display panel of this invention
[Drawing 189] The explanatory view of the display panel of this invention
[Drawing 190] The explanatory view of the display panel of this invention
[Drawing 191] The explanatory view of the display panel of this invention
[Drawing 192] The explanatory view of the display panel of this invention

[Drawing 193] The explanatory view of the display panel of this invention
[Drawing 194] The explanatory view of the display panel of this invention
[Drawing 195] The explanatory view of the display panel of this invention
[Drawing 196] The explanatory view of the display panel of this invention
[Drawing 197] The explanatory view of the display panel of this invention
[Drawing 198] The explanatory view of the drive approach of the display panel of this invention
[Drawing 199] The explanatory view of the drive approach of the display panel of this invention
[Drawing 200] The explanatory view of the drive approach of the display panel of this invention
[Drawing 201] The explanatory view of the drive approach of the display panel of this invention
[Drawing 202] The explanatory view of the drive approach of the display panel of this invention
[Drawing 203] The explanatory view of the display panel of this invention
[Drawing 204] The explanatory view of the information display of this invention
[Drawing 205] The explanatory view of the information display of this invention
[Drawing 206] The explanatory view of the information display of this invention
[Drawing 207] The explanatory view of the drive approach of the display of this invention
[Drawing 208] The explanatory view of the drive approach of the display of this invention
[Drawing 209] The explanatory view of the drive approach of the display of this invention
[Drawing 210] The explanatory view of *********** of this invention
[Drawing 211] The explanatory view of the display panel of this invention
[Drawing 212] The explanatory view of the display panel of this invention
[Drawing 213] The explanatory view of the display panel of this invention
[Drawing 214] The explanatory view of the display panel of this invention
[Drawing 215] The explanatory view of the drive approach of the display panel of this invention
[Drawing 216] The explanatory view of the drive approach of the display panel of this invention
[Drawing 217] The explanatory view of the drive approach of the display panel of this invention
[Drawing 218] The explanatory view of the drive approach of the display panel of this invention
[Drawing 219] The explanatory view of the drive approach of the display panel of this invention
[Drawing 220] The explanatory view of the drive approach of the display panel of this invention
[Drawing 221] The explanatory view of the display panel of this invention
[Drawing 222] The explanatory view of the display panel of this invention
[Drawing 223] The explanatory view of the display panel of this invention
[Drawing 224] The explanatory view of the display panel of this invention
[Drawing 225] The explanatory view of the display panel of this invention
[Drawing 226] The explanatory view of the display panel of this invention
[Drawing 227] The explanatory view of the display panel of this invention
[Drawing 228] The explanatory view of the display panel of this invention
[Drawing 229] The explanatory view of the display panel of this invention
[Drawing 230] The explanatory view of the display panel of this invention
[Drawing 231] The explanatory view of the display panel of this invention

[Drawing 232] The explanatory view of the display panel of this invention
[Drawing 233] The explanatory view of the display panel of this invention
[Drawing 234] The explanatory view of the display panel of this invention
[Drawing 235] The explanatory view of the display panel of this invention
[Drawing 236] The explanatory view of the display panel of this invention
[Drawing 237] The explanatory view of the display panel of this invention
[Drawing 238] The explanatory view of the display panel of this invention
[Drawing 239] The explanatory view of the display panel of this invention
[Drawing 240] The explanatory view of the display panel of this invention
[Drawing 241] The explanatory view of the display panel of this invention
[Drawing 242] The explanatory view of the display panel of this invention
[Drawing 243] The explanatory view of the display panel of this invention
[Drawing 244] The explanatory view of the display panel of this invention
[Drawing 245] The explanatory view of the display panel of this invention
[Drawing 246] The explanatory view of the display panel of this invention
[Drawing 247] The explanatory view of the display panel of this invention
[Drawing 248] The explanatory view of the display panel of this invention
[Drawing 249] The explanatory view of the display panel of this invention
[Drawing 250] The explanatory view of the display panel of this invention
[Drawing 251] The explanatory view of the display panel of this invention
[Drawing 252] The explanatory view of the display panel of this invention
[Drawing 253] The explanatory view of the display panel of this invention
[Drawing 254] The explanatory view of the display panel of this invention
[Drawing 255] The explanatory view of the display panel of this invention
[Drawing 256] The explanatory view of the display panel of this invention
[Drawing 257] The explanatory view of the display panel of this invention
[Drawing 258] The explanatory view of the display panel of this invention
[Drawing 259] The explanatory view of the display panel of this invention
[Drawing 260] The explanatory view of the display panel of this invention
[Drawing 261] The explanatory view of the display panel of this invention
[Drawing 262] The explanatory view of the display panel of this invention
[Drawing 263] The explanatory view of the display panel of this invention
[Drawing 264] The explanatory view of the display panel of this invention
[Drawing 265] The explanatory view of the display panel of this invention
[Drawing 266] The explanatory view of the display panel of this invention
[Drawing 267] The explanatory view of the display panel of this invention
[Drawing 268] The explanatory view of the display panel of this invention
[Drawing 269] The explanatory view of the display panel of this invention
[Drawing 270] The explanatory view of the display panel of this invention
[Drawing 271] The explanatory view of the display panel of this invention
[Drawing 272] The explanatory view of the display panel of this invention
[Drawing 273] The explanatory view of the display panel of this invention
[Drawing 274] The explanatory view of the display panel of this invention
[Drawing 275] The explanatory view of the display panel of this invention
[Drawing 276] The explanatory view of the display panel of this invention
[Drawing 277] The explanatory view of the display panel of this invention
[Drawing 278] The explanatory view of the display panel of this invention
[Drawing 279] The explanatory view of the display panel of this invention
[Drawing 280] The explanatory view of the display panel of this invention
[Drawing 281] The explanatory view of the display panel of this invention

[Description of Notations]
11 TFT
12 Gate Driver
14 Source Driver
15 EL Element
16 Pixel
17 Gate Signal Line
18 Source Signal Line
19 Capacitor (Storage Capacitance, Capacitor)
20 Current Supply Source Line (Electric Power Supply Line, Electrical-Potential-Difference Supply Line)
21 Viewing Area (Display Screen, Effective Viewing Area)
23 Laser Radiation Spot
41 Closure Free Wheel Plate (Sealing Agent)
43 44 Heights
45 Sealing Compound (**)
46 Reflective Film
47 Organic Electroluminescence (EL Element)
48 Pixel Electrode
49 Array Substrate
50 Lambda/4 Plate (Lambda/4 Sheet)
51 Cathode Wiring
52 Contact
53 Cathode
54 Polarizing Plate
55 Drying Agent (Dry Material, Moisture Absorption Means)
61 62 Connection terminal
63 Anode
71 Smoothing Film

72 Transparent Electrode
73 Closure Film
74 Circular Polarization of Light Plate
81 Edge Protective Coat
91 Light-shielding Film
92 Low Resistance-ized Wiring (Metal Membrane)
101 Control IC
102 Power Source IC
103 Printed Circuit Board
104 Flexible Substrate
105 Data Signal
141 Error Diffusion Controller
151 Built-in Display Memory
152 Operation Memory
153 Arithmetic Circuit
154 Buffer Circuit
191 Antenna
192 Ten Key
193 Case
194 Carbon Button
201 Day PUREKUSA
202 LNA
203 LO Buffer
204 Down Converter
205 Up Converter
206 PA PURIDORAIBA
207 PA
241 Glass Substrate
242 Positioning Marker
251 Heights
252 Concave Heights (Embossing Section)
14a 1 chip driver IC
311 Image Display Field
312 Non-display Field
351 Counter Circuit
352 Brightness Memory
353 CPU
354 Frame (Field Memory, SRAM)
355 Change Circuit
391 Write-in Pixel Line
392 Maintenance Pixel Line
401 Voltage Source
402 Current Source
403 Power-Source Change Means
404 Stray Capacity (Parasitic Capacitance)
451 Body
452 Eyepiece Ring
453 Magnifying Lens
454 Positive Lens
461 Taking Lens

462 Body of Video Camera
463 Storing Section
464 Eyepiece Covering
465 Display-Mode Changeover Switch
466 Lid (Cover)
467 Supporting Point
471 Shutter
472 Body of Digital Camera (Electronic Camera)
481 Outer Frame
482 Holddown Member
483 Foot
484 Foot Installation Section
491 Wall
492 Fixed Metallic Ornaments
493 Protection Film (Guard Plate, Safeguard)
501 Scan Field
601 ENBL Terminal (Control Terminal)
602 OR Circuit
851 Shutter (Protection-from-Light Means)
852 Glasses (Change Means)
871 Write-in Pixel Line
1221 Voltage-Output Circuit
1222 Current Output Circuit
1223 Change Circuit (Analog Switch)
1224 Operational Amplifier (Output Buffer)
1225 Adjustment BORIUMU (Variable Resistance, Adjustment Device)
1226 DA Converter (Digital-to-Analog Means (Vessel))
1227 Output Transistor (Transistor, FET)
1228 Resistance
1321 Signal Wiring
1751 Pixel Contact Section
1761 Protective Coat (Layer)
1781 Spacer
1791 Lighting Control Line
1981 Block (Unit)
2041 Loudspeaker
2043 Function Switch (FSW)
2044 Microphone
2045 Mirror (Mirror)
2046 Display Panel (Display)
2111 Reverse Bias Control Line
2561 Insulator Layer
2621 2681 Frame (field) memory
2622 Counter Circuit
2623 Data-Conversion Circuit
2682 Adder Circuit (Data-Processing Circuit)
2683 Gate Driver Control Circuit
2691 Data Control Circuit
2692 Data-Conversion Circuit
2751 Bias Resistance (Electronic BORIUMU, Current Modification Means)

2752 Switch Transistor (Selecting Switch)
2753 Parent Transistor
2754 Child Transistor
2791 Light (Locus)
2801 Refraction Sheet (Plate, Film)
2802 Refraction Section
2861 Transparent Membrane
2862 Roller
2863 Concave Heights (Crevice)
2871 Heights
2881 Metal Mask
2901 Press Plate (Pressure-Welding Means, Imprint Means)
2902 Light (UV Light, Light)
3001 Current Sampling Circuit
3002 Current Program Line
3271 Buffer Circuit
3272 OR Circuit
3491 Decoder Circuit
3511 Precharge Circuit
3521 Data Shift Circuit
3661 Bank
3662 2nd Pixel Electrode